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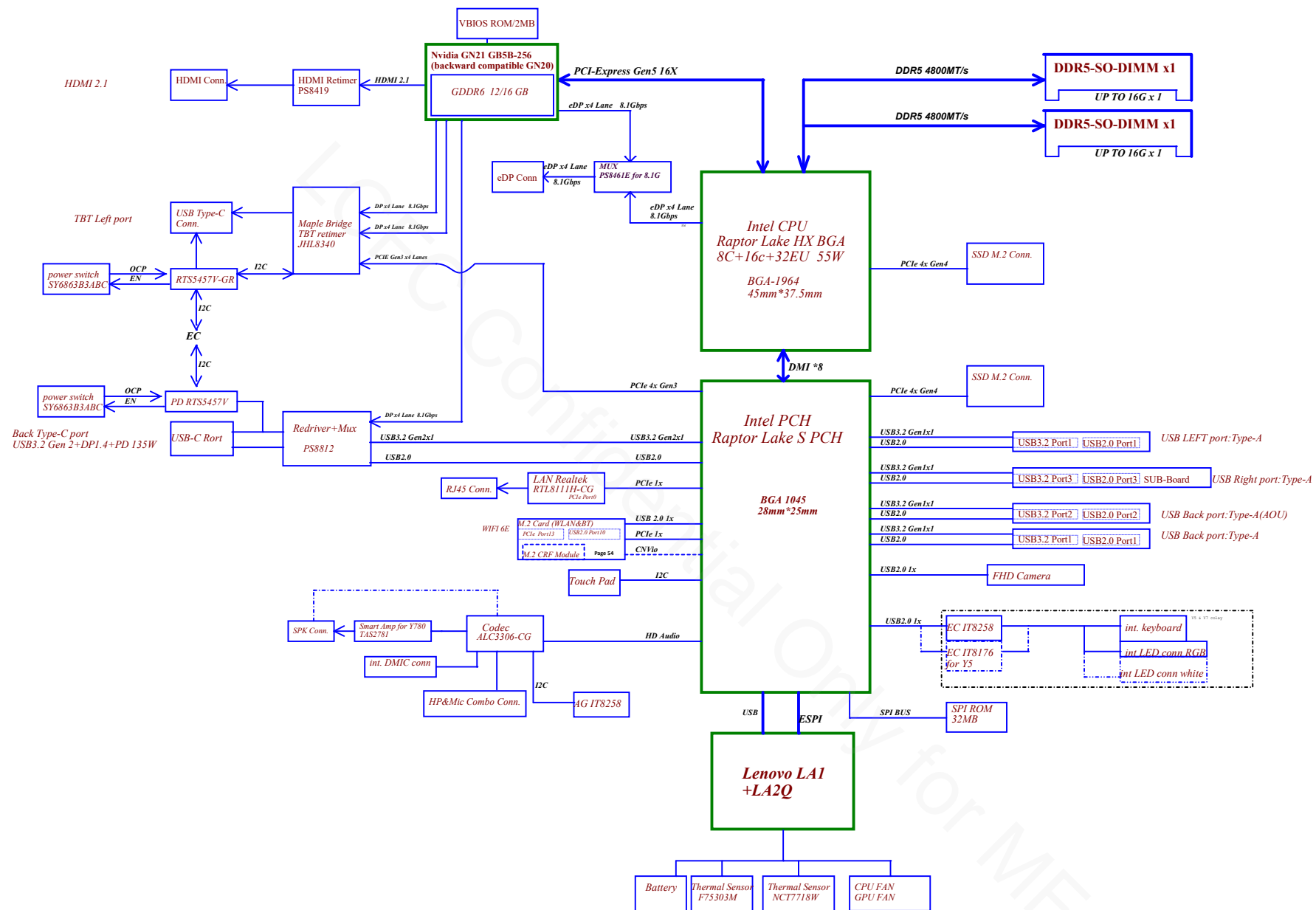
Yx80 GN21 MB1 Schematics Document

Raptor Lake-Hx H55-Processor with DDR5 + NV GN21 GPU

2022-08-11

REV: 0.1

Security Classification		LCFC Highly Confidential Information		Title		Cover Page		LCFC	
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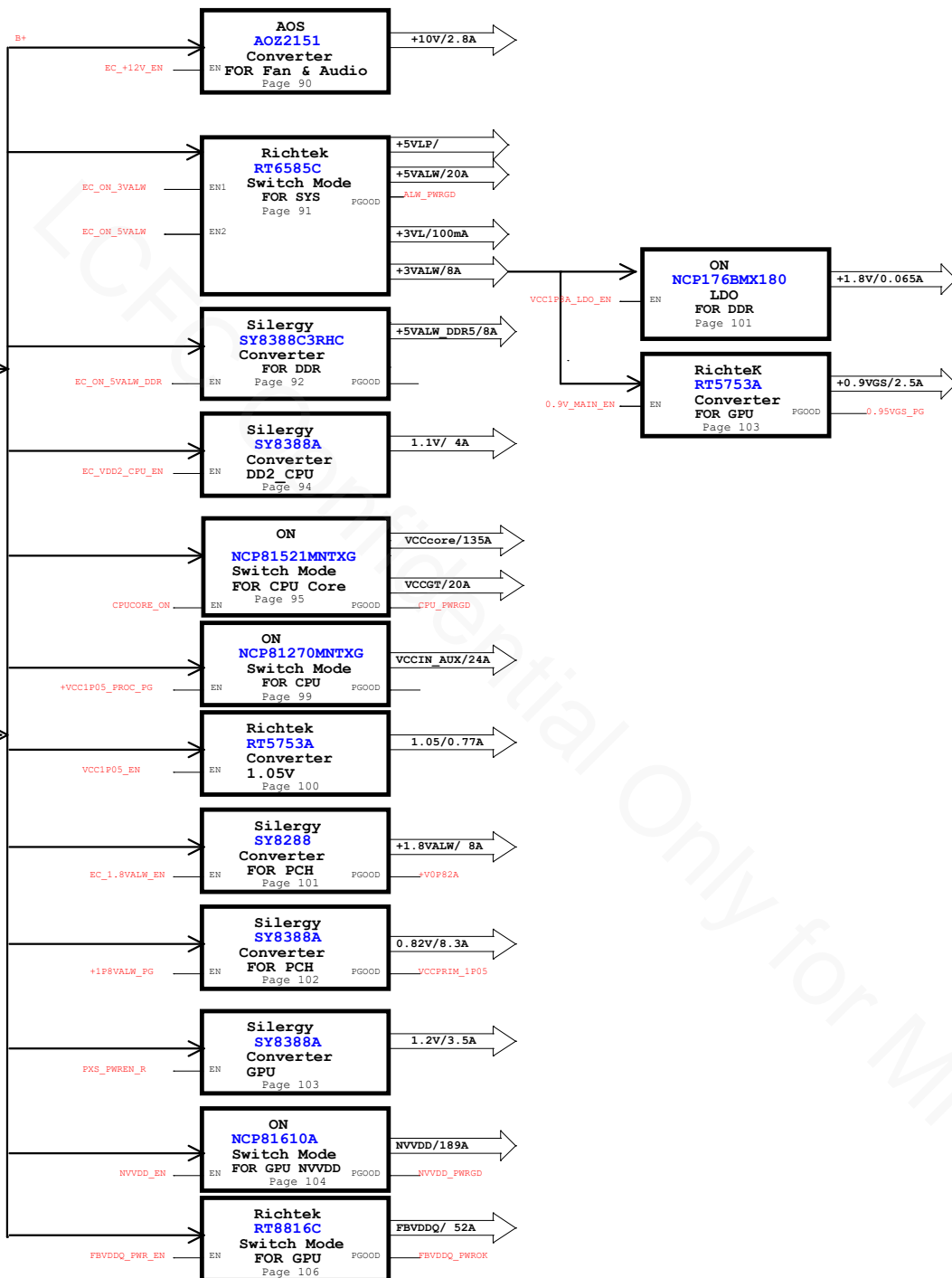
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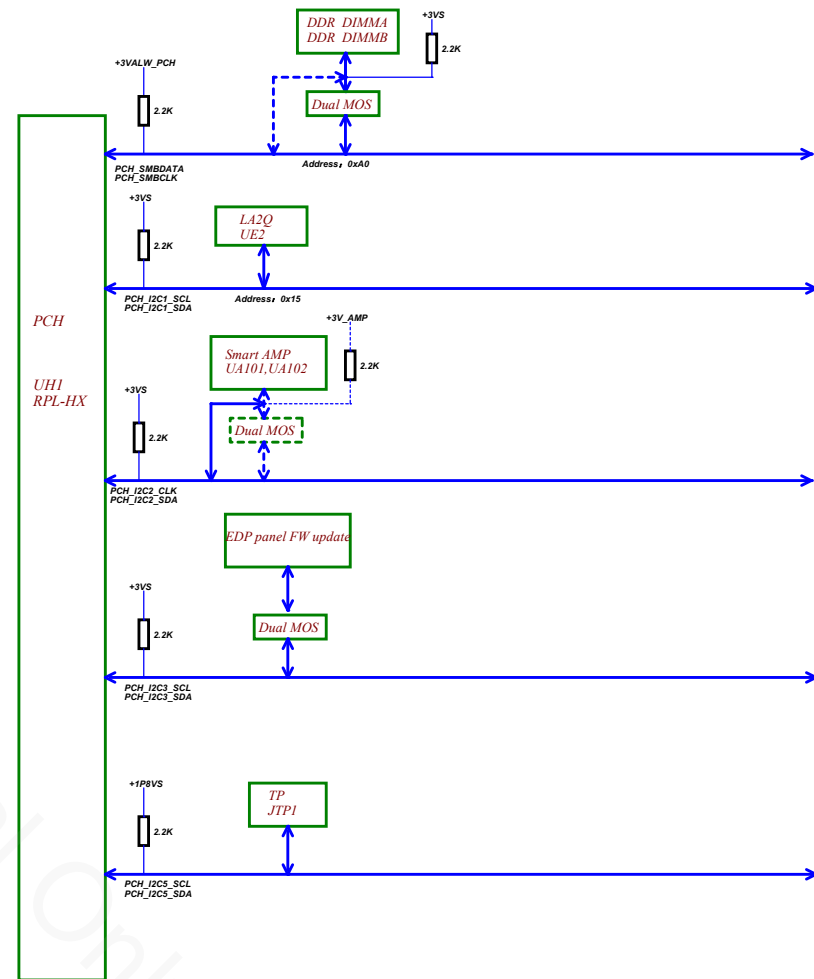
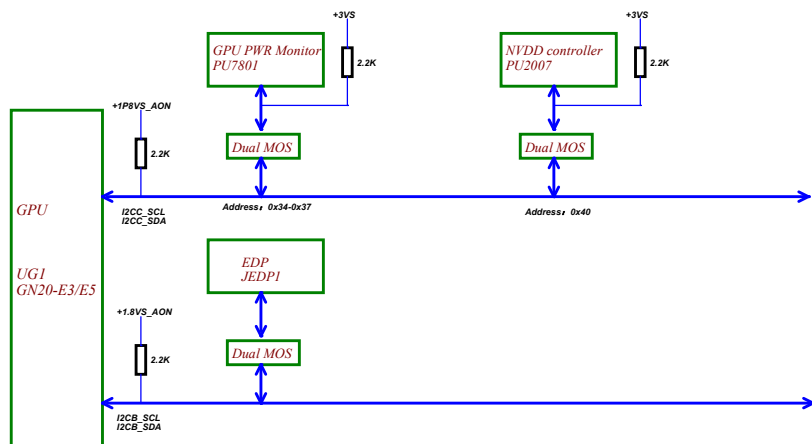
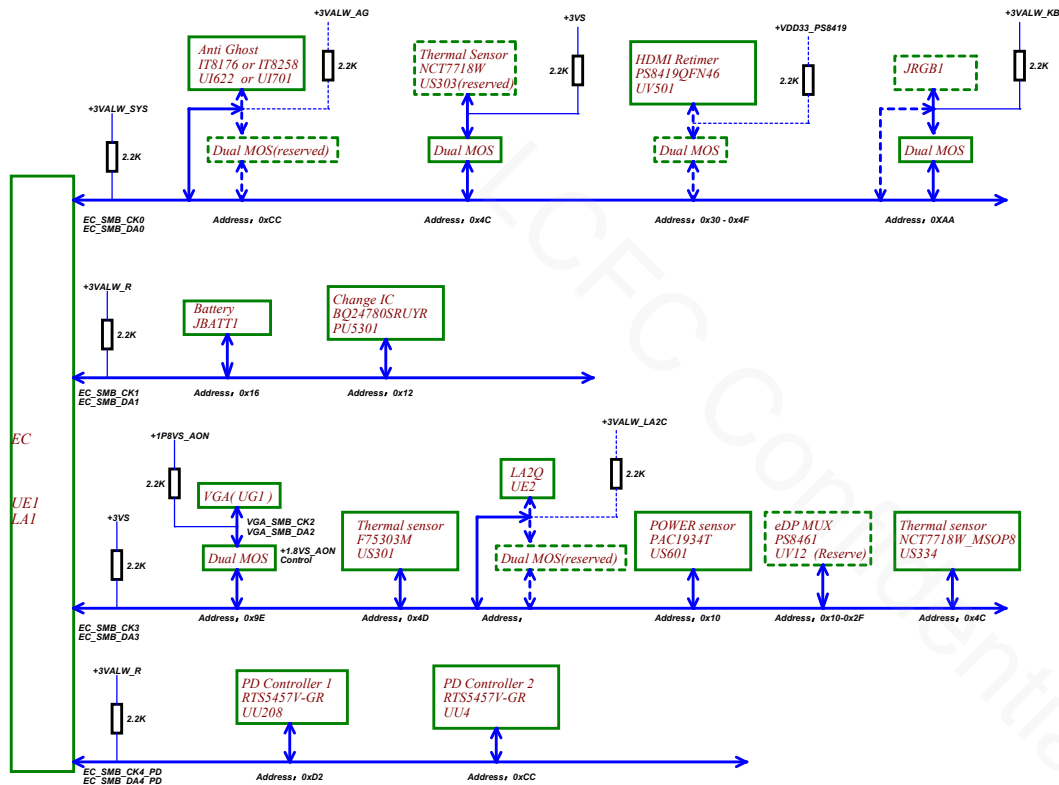
Adaptor
135W/TYPEC
300/330W/Wall-Plug

TI
BQ24780S
Battery Charger
Switch Mode
Page 89

SMBus

Battery
Li-ion
80Wh

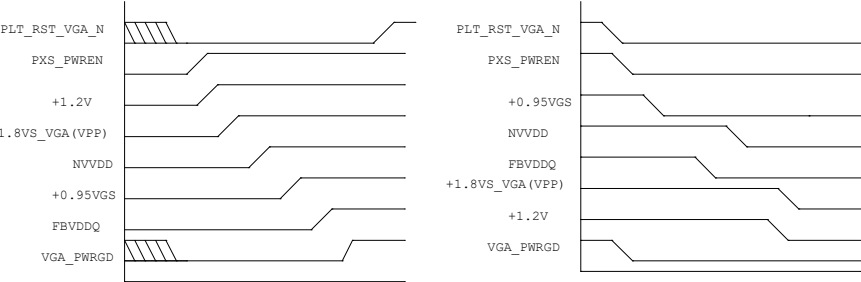




GN21 GPIO

GPIO	I/O	GPIO Name	Function Description	Net name	I/O Termination
GPIO0	OUT	NVVD_PWM_VID	PWM Output to control NVVDD	NVVD_PWM_VID	
GPIO1	OUT	GC6:GC6_FB_EN	FB Enable for GC6	FB_GC6_EN	(10K PD)
GPIO2	IN	GC6:GPU_EVENT*	Wake the GPU from GC6 state	GPU_EVENT#_R	(10K PU)
GPIO3	OUT	DISP_MUX_CNTL	Display MUX control signal	GPU_MUX_CNTL	(10K PD)
GPIO4	OUT	GC6:NVVD_EN	GPU power sequencing for GC6 ---NVVD_EN	GPIO4_GC6_NVVD_EN	(10K PU)
GPIO5	OUT	FRAME_LOCK*	Active low Frame Lock for NVSR panel	UNUSED	
GPIO6	OUT	NVVD_PSI*	Phase Shedding, NVVD_PSI	NVVD_PSI	(10K PU) RSVD
GPIO7	OUT	LCD_BL_PWM	LCD Panel Backlight PWM	GPU_EDP_PWM	(100K PD)
GPIO8	OUT	MEM_VDD_CTL	Memory voltage Control	FBVDDQ_SEL	(10K PD)
GPIO9	I/O	THERM_ALERT*	Active Low Thermal Alert	VGA_ALERT#	(10K PU)
GPIO10	OUT	MEM_VREF_CTL	Memory VREF Control	MEM_VREF_CTL	(100K PD)
GPIO11	OUT	LCD_VDD	LED Panel power enable	GPU_EDP_ENVVD	(10K PD)
GPIO12	IN	PWR_LEVEL	AC power detect or power supply overdraw input	VGA_AC_DET_R	(10K PU)
GPIO13	IN	IGPU_BL_EN	Signal indicating when the IGPU has EN the BL	IGPU_EDP_ENBKL	(100K PU)
GPIO14	IN	HPD_IFPE*	Hot Plug Detect for IFPE	IFPD_HPD	(10K PU)
GPIO15	IN	UNUSED		UNUSED	
GPIO16	OUT	DISP_MUX_PWM_CNTL	Allows switching the PWM between IGPU & DGPU	PWM_SW_SELECT	(10K PD)
GPIO17	IN	HPD_IFPB*	Hot Plug Detect for IFB	GPU_EDP_HPD	(10K PU)
GPIO18	IN	HPD_IFPC*	Hot Plug Detect for IFPC	LNK1_HPD	(10K PU)
GPIO19	OUT	UNUSED			
GPIO20	OUT	UNUSED			
GPIO21	OUT	LCD_BLEN	LCD Panel Backlight Enable	GPU_EDP_ENBKL	(100K PD)
GPIO22	OUT	ADC_MUX_SEL	OVRM MUX Input SEL	ADC_MUX_SEL	(2.2K PU)
GPIO23	OUT	UNUSED	UNUSED		
GPIO24	IN	HPD_IFPD*	Hot Plug Detect for IFPD	LNK2_HPD	(10K PU)
GPIO25	OUT	FBVDD_PSI	Turns off phases of the Frame buffer power supply	FBVDDQ_PSI	(5.1K PU)
GPIO26	OUT	ROM_WP* FP_FUSE N18P-G61-A Control FP_FUSE	Connect to WP pin of the GPU EEPROM	GPIO26_ROM_WP GPIO26_FP_FUSE	(10K PD) (10K PD) RSVD
GPIO27	IN	HPD_IFPA*	Hot Plug Detect for IFPA	IFPA_HPD	(10K PU)
GPIO28	OUT	UNUSED		UNUSED	
GPIO29	OUT	UNUSED		UNUSED	
GPIO30	OUT	UNUSED		UNUSED	

GN21 Power Sequence



1. The ramp time for any rail must be more than 40us and is recommended to be less than 2ms.
2. It is recommended that the delay from I18 on to PEXVDD/GPU_P0OOD assertion not exceed 20ms.
- 3.The ramp-up overshoot should not exceed the silicon reliability limit voltage.
4. Power up NVVD must be 90s before PEXVDD can ramp-up.
5. Refer to the JEDEC Memory SPEC for memory-related power sequencing.
7. FBVDD/Q, USB_VDDP and I18_AON don't need power cycle for GC6

1. For GDDR6, VFP must be equal to or higher than FBVDD/Q at all times;use gate logic and discharge circuit as needed
2. All 3.3V devices that connect to the GPU must be ramp down before I18; GPU can NOT have any 3.3V leakage path after I18 power down.
3. Power down of PEXVDD must be less than 10s before NVVD can start ramp-down.

H=High: Tied to 1.8V
M=Middle: Tied to 0.9V
L=Low: Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	GN20x-E VRAM
L	L	L	0 (0x0000)	Samsung K4Z80325BC-HC14
L	L	H	1 (0x0001)	Micron MT61K256M32JE-14:A
L	H	L	2 (0x0002)	Hynix H56C8H24AIR-S2C
L	H	H	3 (0x0003)	
H	L	L	4 (0x0004)	
H	L	H	5 (0x0005)	
H	H	L	6 (0x0006)	
H	H	H	7 (0x0007)	
L	L	M	8 (0x0008)	
L	M	L	9 (0x0009)	Samsung(for E7) K4ZAF325BM-HC 14
L	M	H	10 (0x000A)	
L	H	M	11 (0x000B)	
M	L	L	12 (0x000C)	
M	L	H	13 (0x000D)	

FS_OVERT# FUNCTION

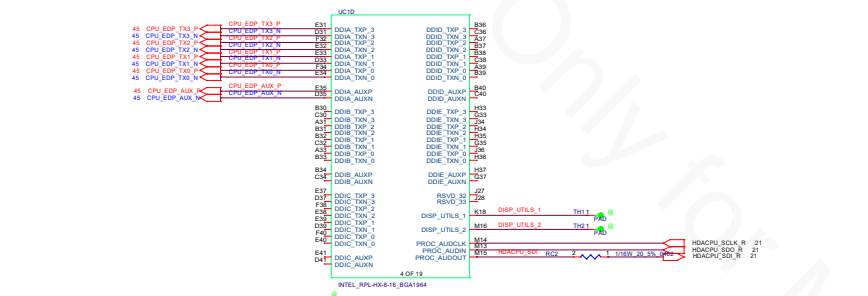
ROM_SO	ROM_SI	ROM_SCLK	FS_OVERT# FUNCTION
L	L	H	FS_OVERT# function ENABLE
L	L	L	FS_OVERT# function DISABLED Reserved; do not configure

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

- 1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
- 1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL
- 1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER
- 1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



For GPU



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Rev		Issued Date		2023/07/01	



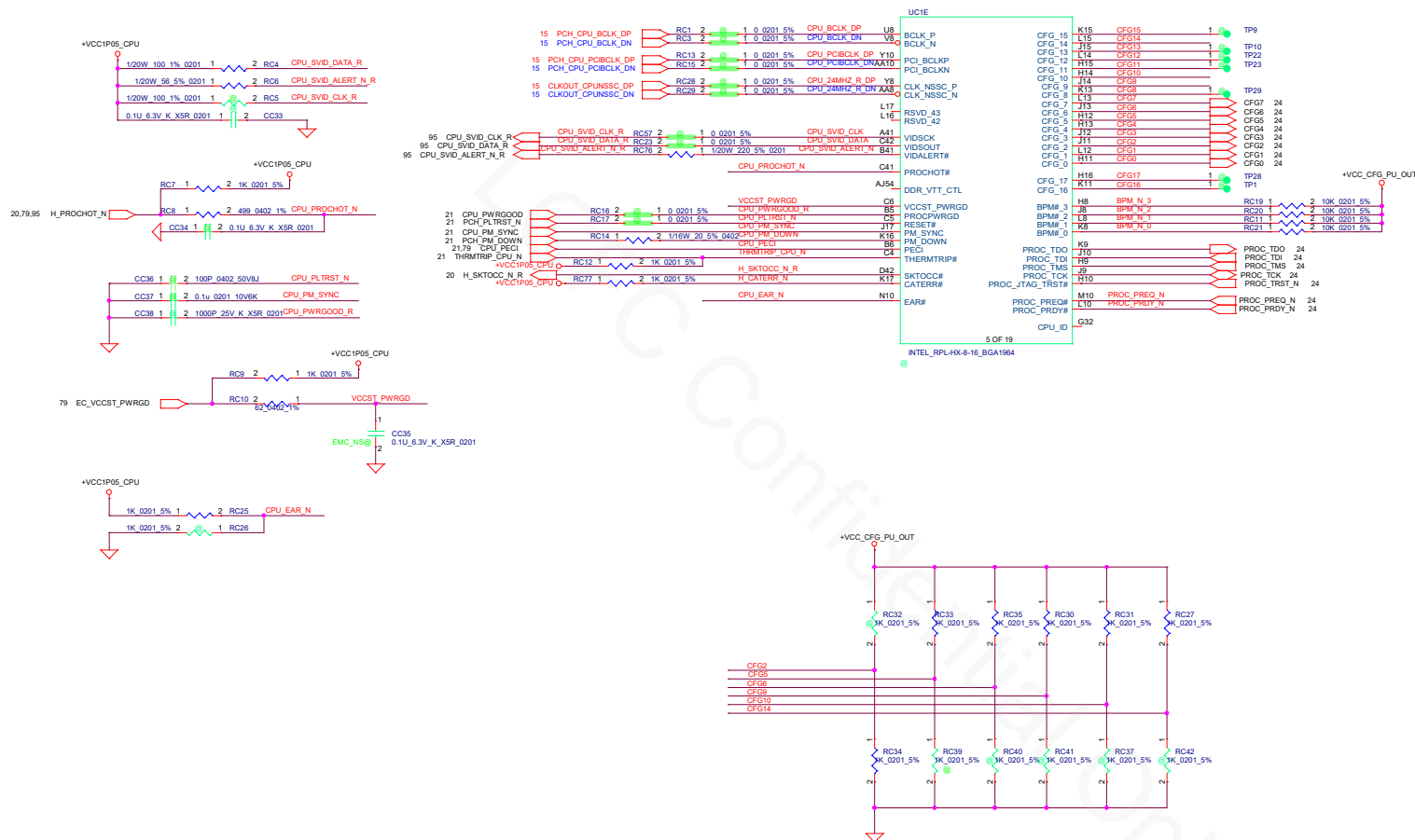
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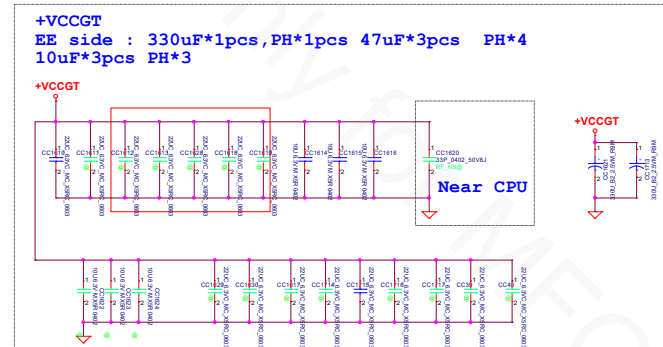
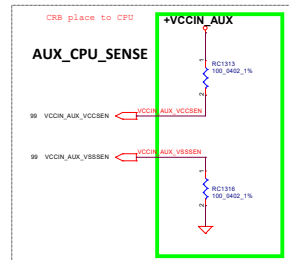
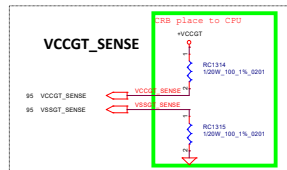
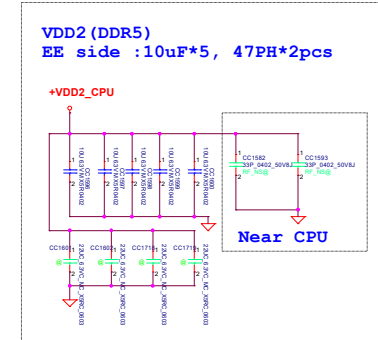
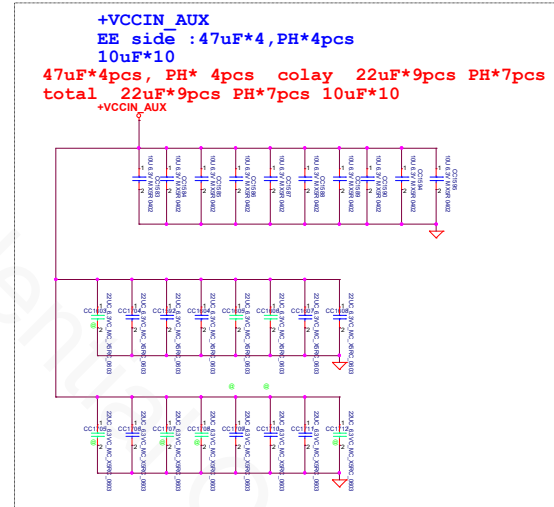
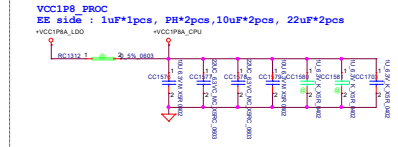
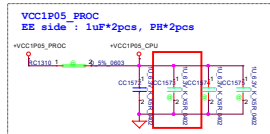
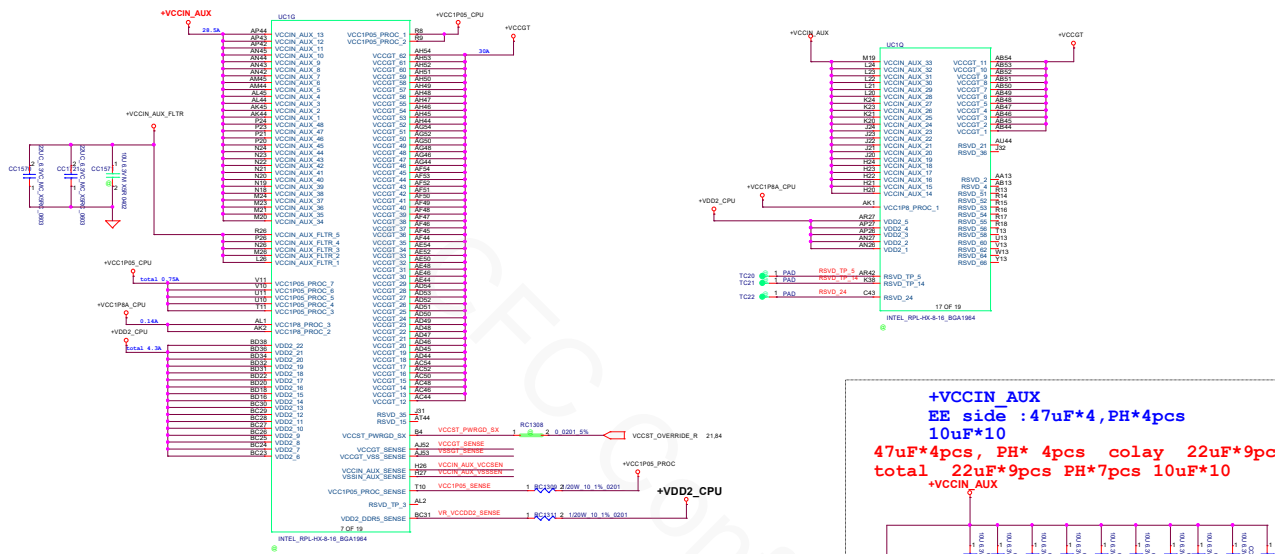
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CFG STRAPS for CPU

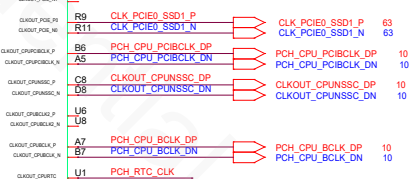
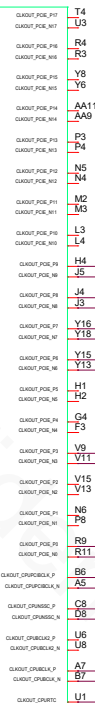
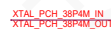
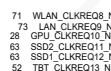


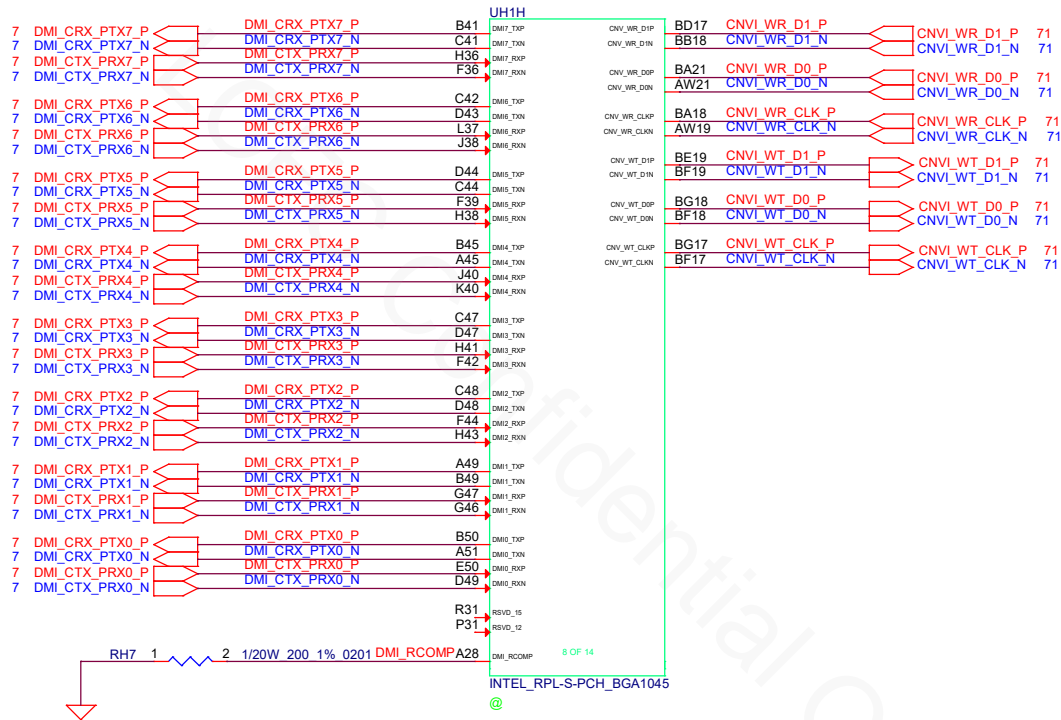
RSVD	
CFG0	N/A
Reserved configuration lane	
CFG1	N/A
PCI Express* Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation ★ 0 = Lane numbers reversed.
Reserved configuration lane	
CFG[3:4]	N/A
PCI Express* Bifurcation	
CFG[5]	★ 1 = 1 x16 PCI Express* 0 = 2 x8 PCI Express*
Reserved configuration lane	
CFG[13:6]	N/A
PEG60 LANE reversal	
CFG14	★ 1 = (default) normal 0 = Reversed
Reserved configuration lane	
CFG[17:15]	N/A

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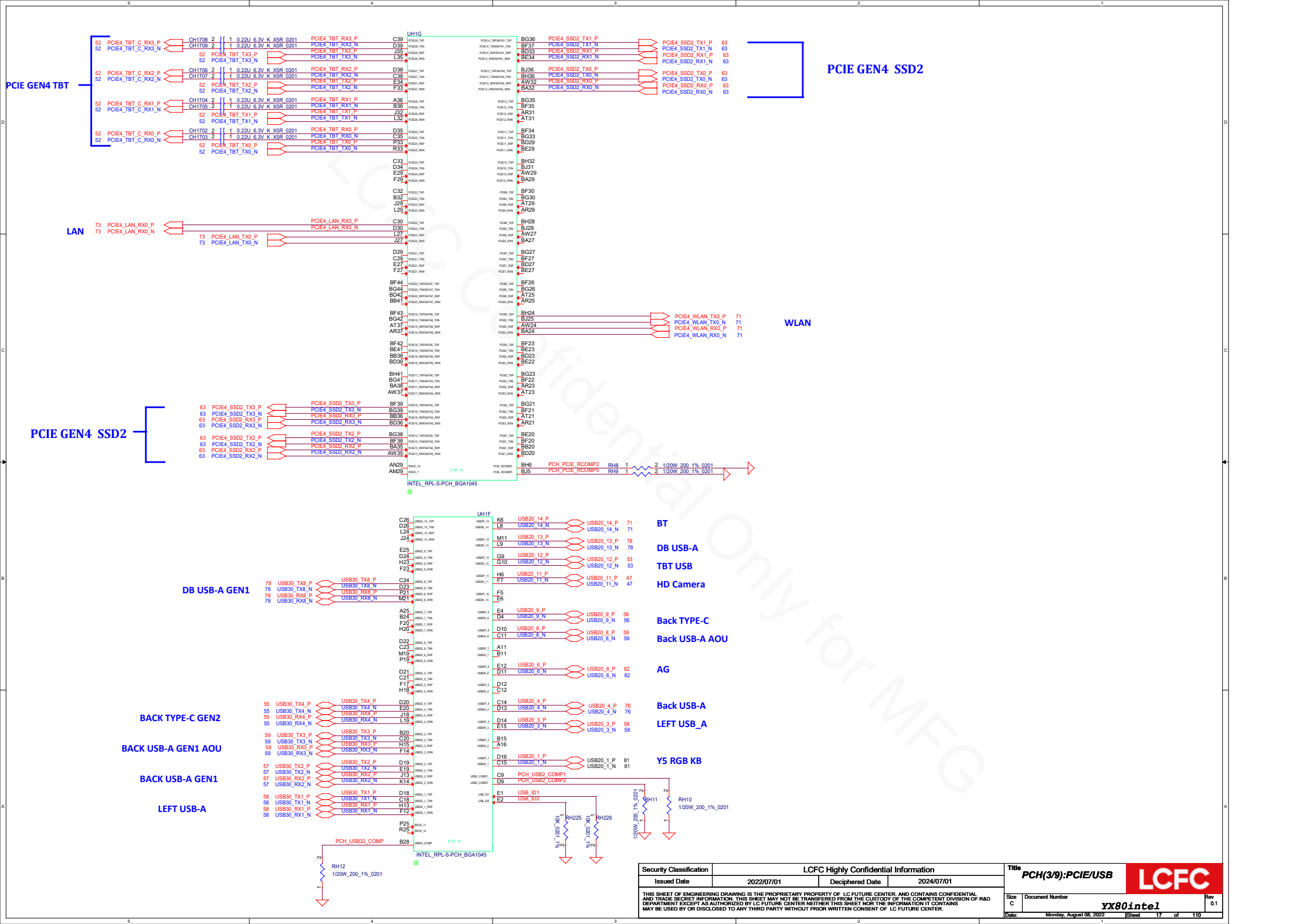


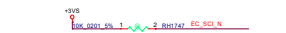
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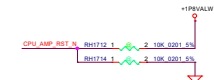
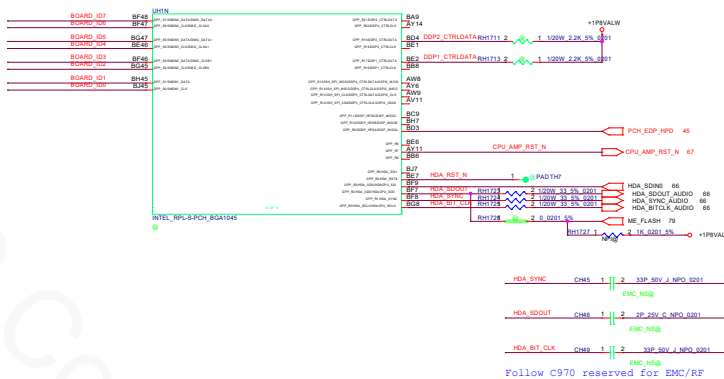




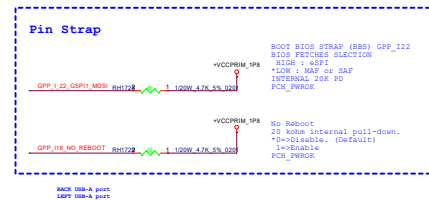
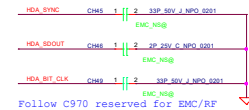
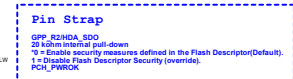
05/28: Check RVP 接法



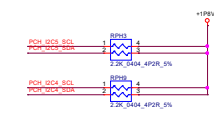
LCD over drive control
OD: low for OD off(*Default)
High for OD on

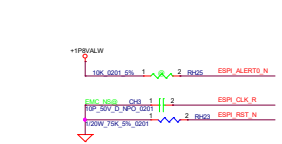


1.8V level

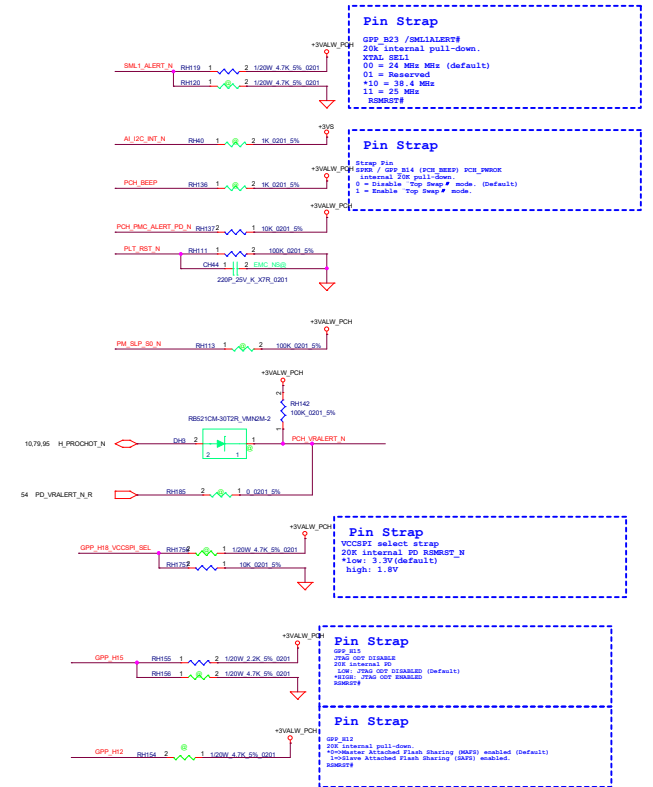
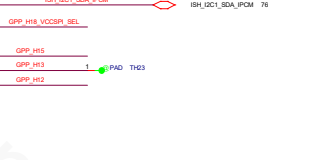
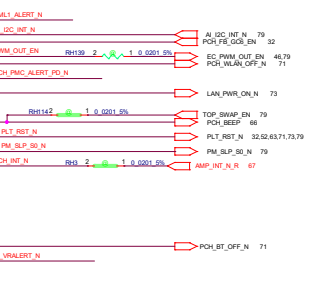
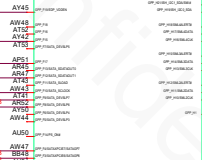
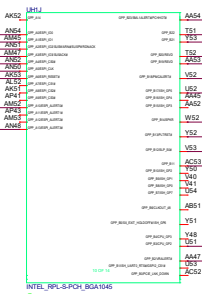
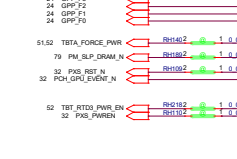
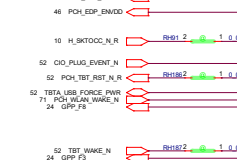
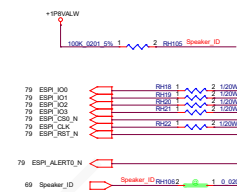
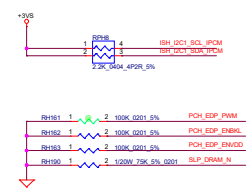
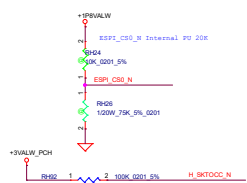


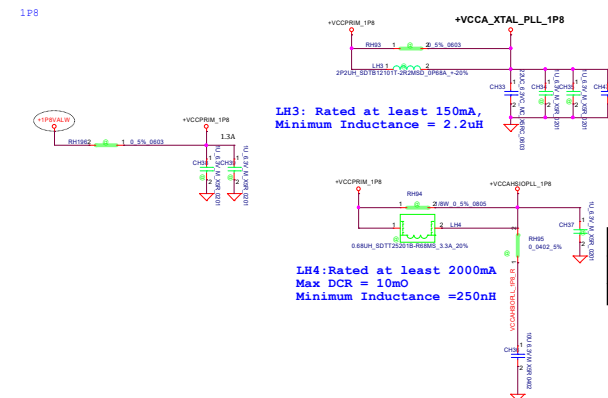
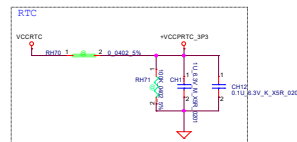
Touchpad 1.8V
panel FW update



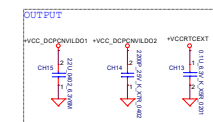
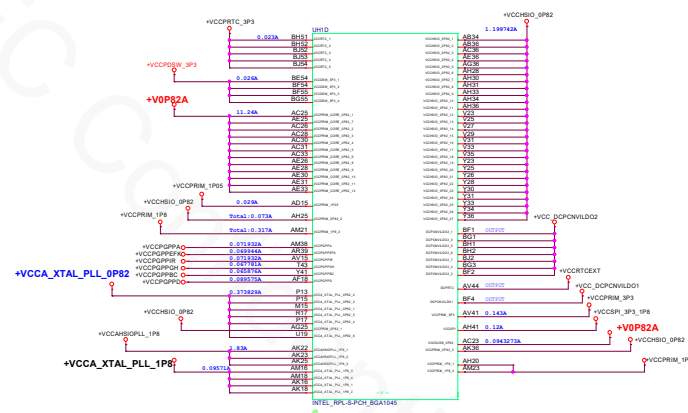
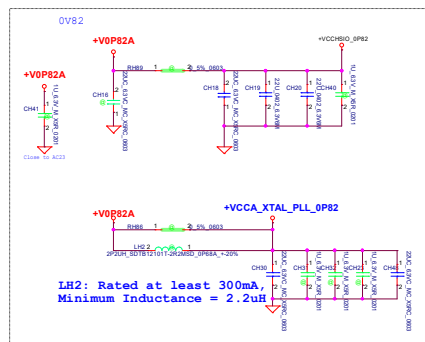


1.8V GPIO

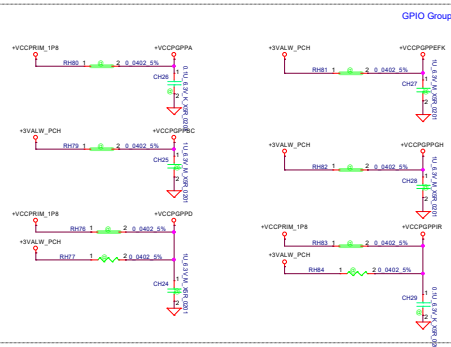




680nF (Placeholder)	1	Inductor by default is a split inductor. If drafted, the inductor needs to have 1000 turns and be rated at least 100mA, DCR: 0.01 ohms +/- 10%
0 ohm_0402 100 mohm_0402	1	Option 1: staff with 0 ohm if the inductor is not drafted Option 2: staff 100 mohm if the inductor is drafted
10u_0402	1	Place the capacitor in package pin D015 and D022 right after the signal trace



GPIO Group	Power Supply
GPP_A/eSPI	1.8 V or 3.3 V
GPP_B/C	1.8 V or 3.3 V
GPP_D	1.8 V or 3.3 V
GPP_E/F/K	1.8 V or 3.3 V
GPP_G/H	1.8 V or 3.3 V
GPP_I/R	1.8 V or 3.3 V
GPP_J	VCCPRIM_1P8
GPP_S	VCCPRIM_1P8
GPD	VCCDSW_3P3



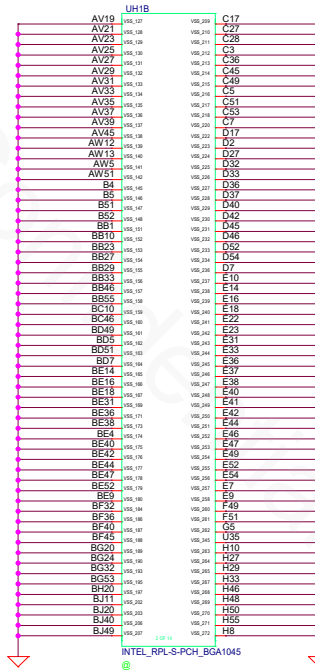
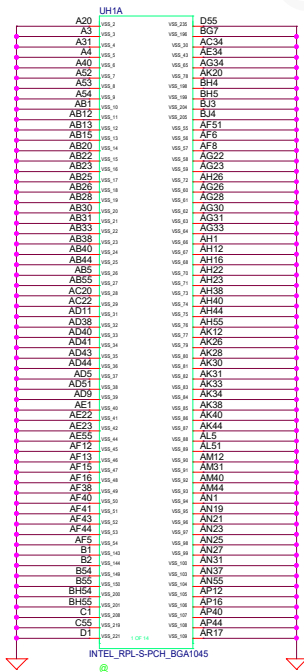
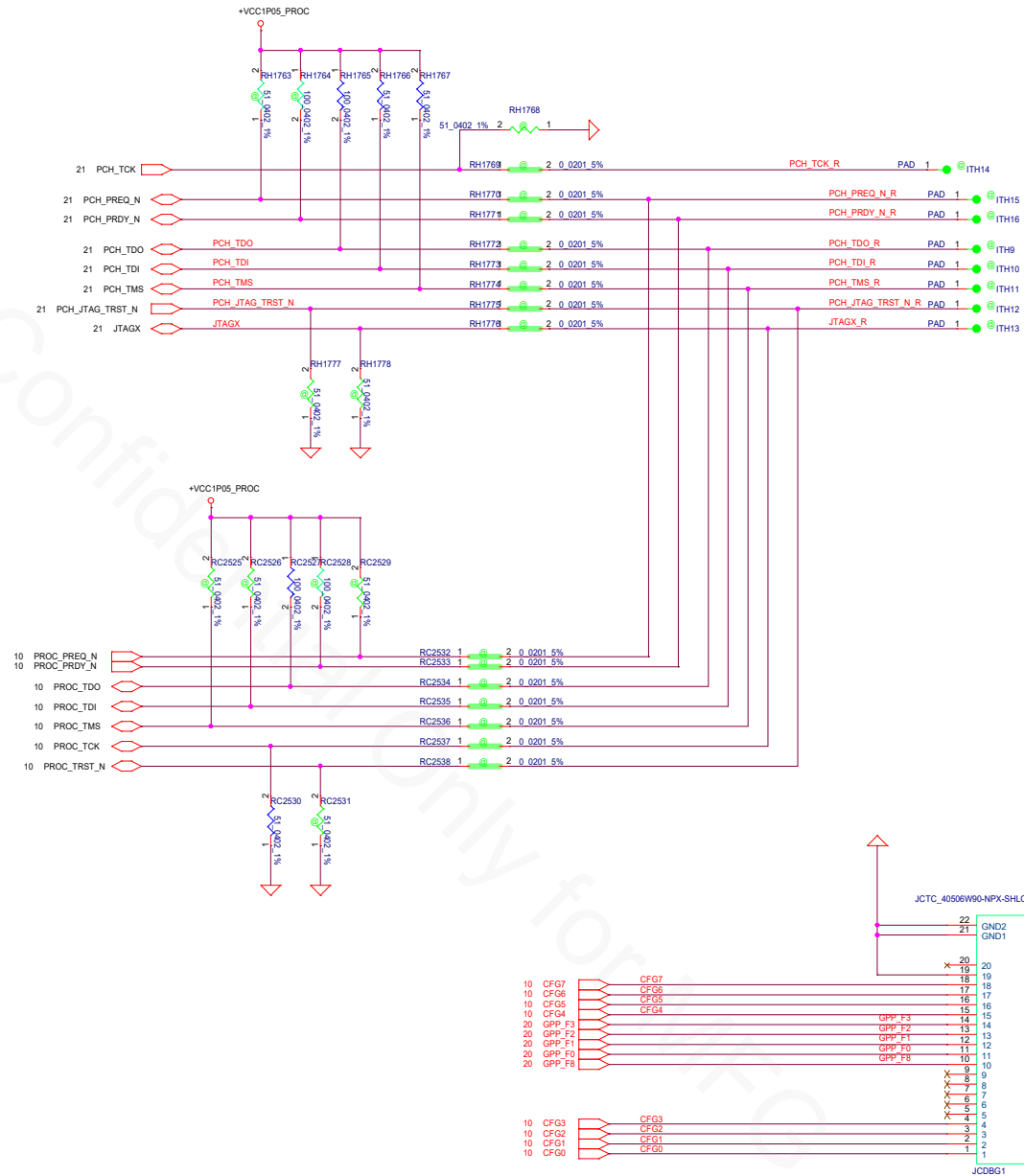
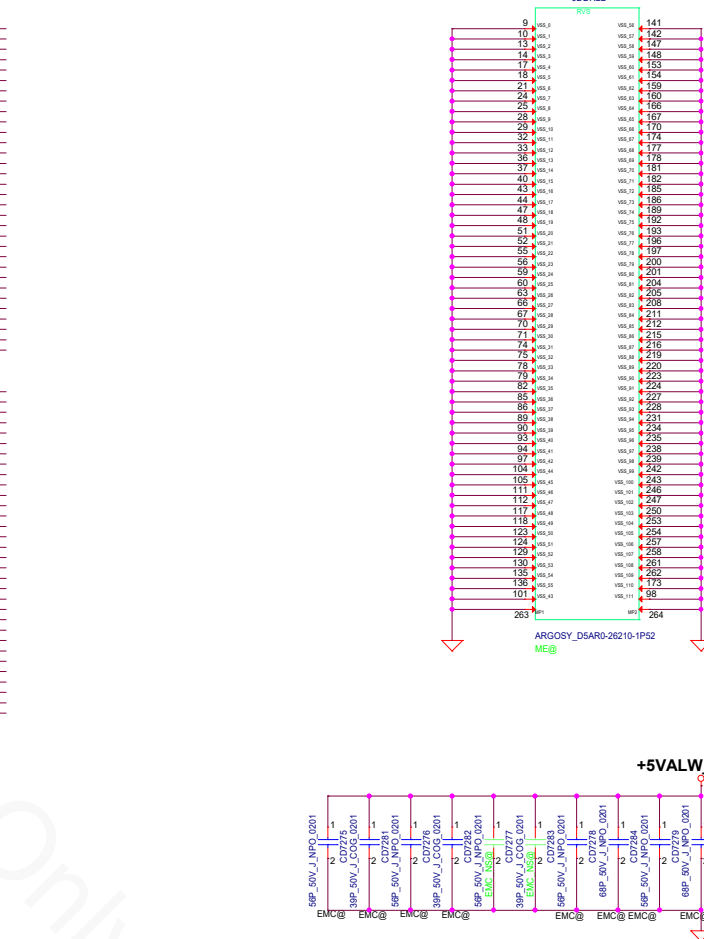
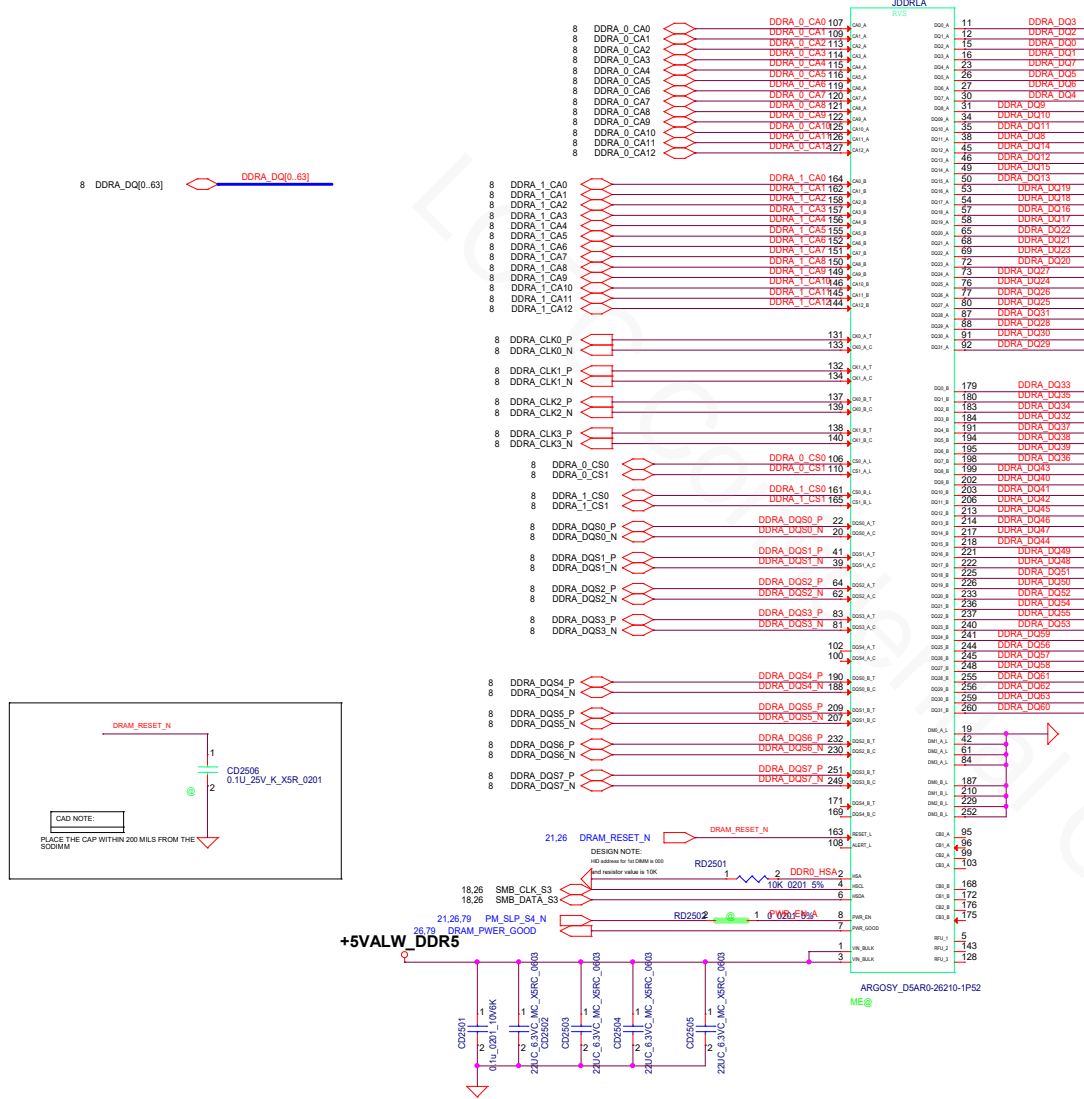
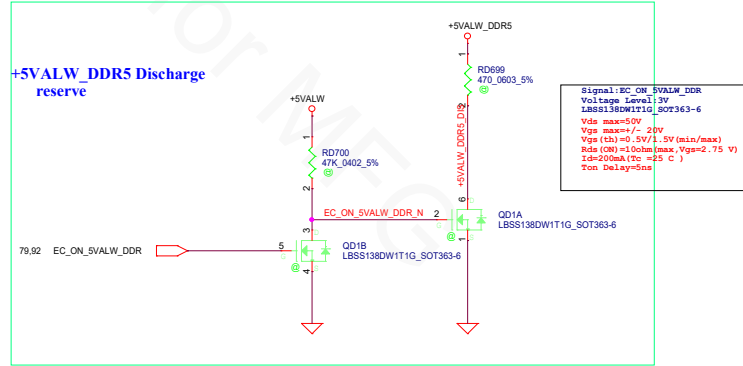



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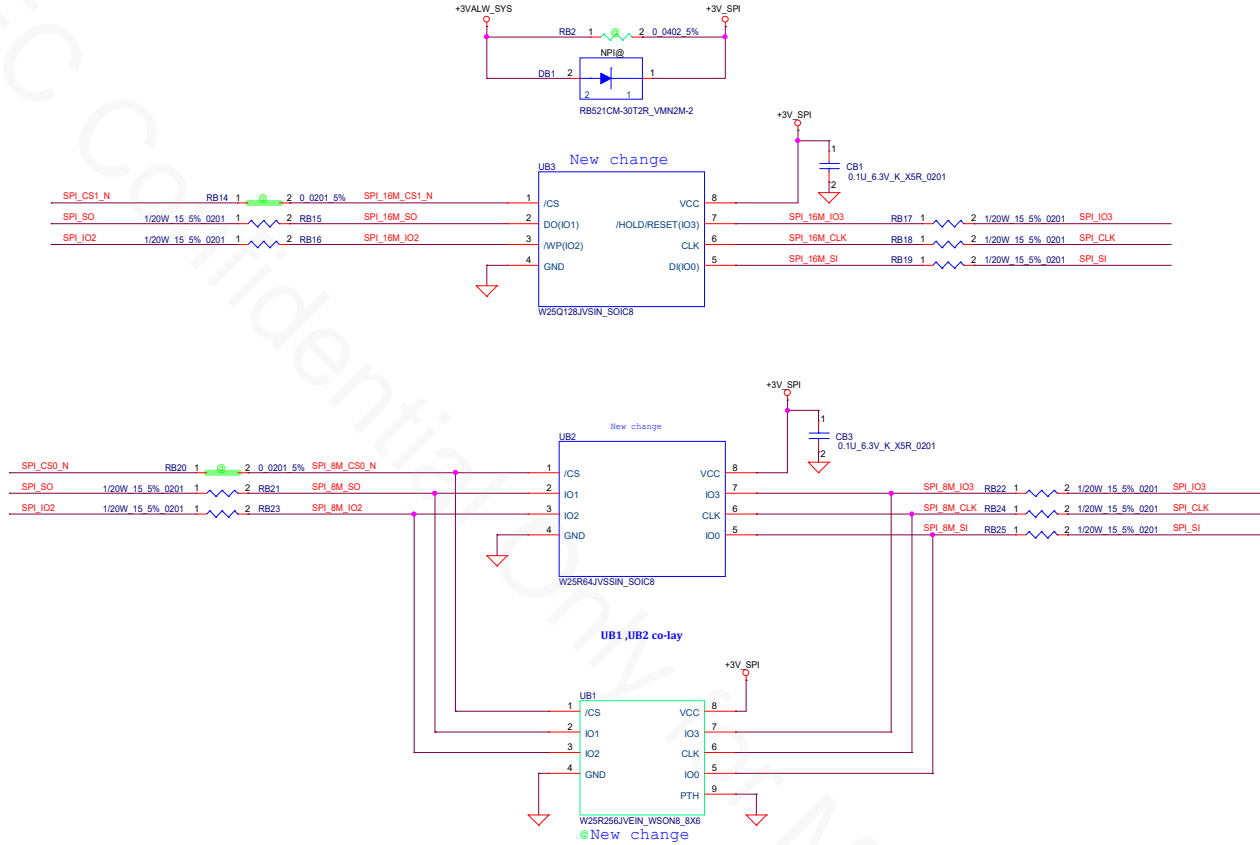
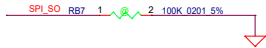
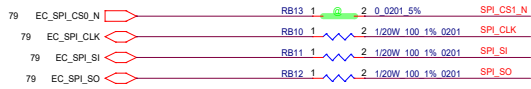
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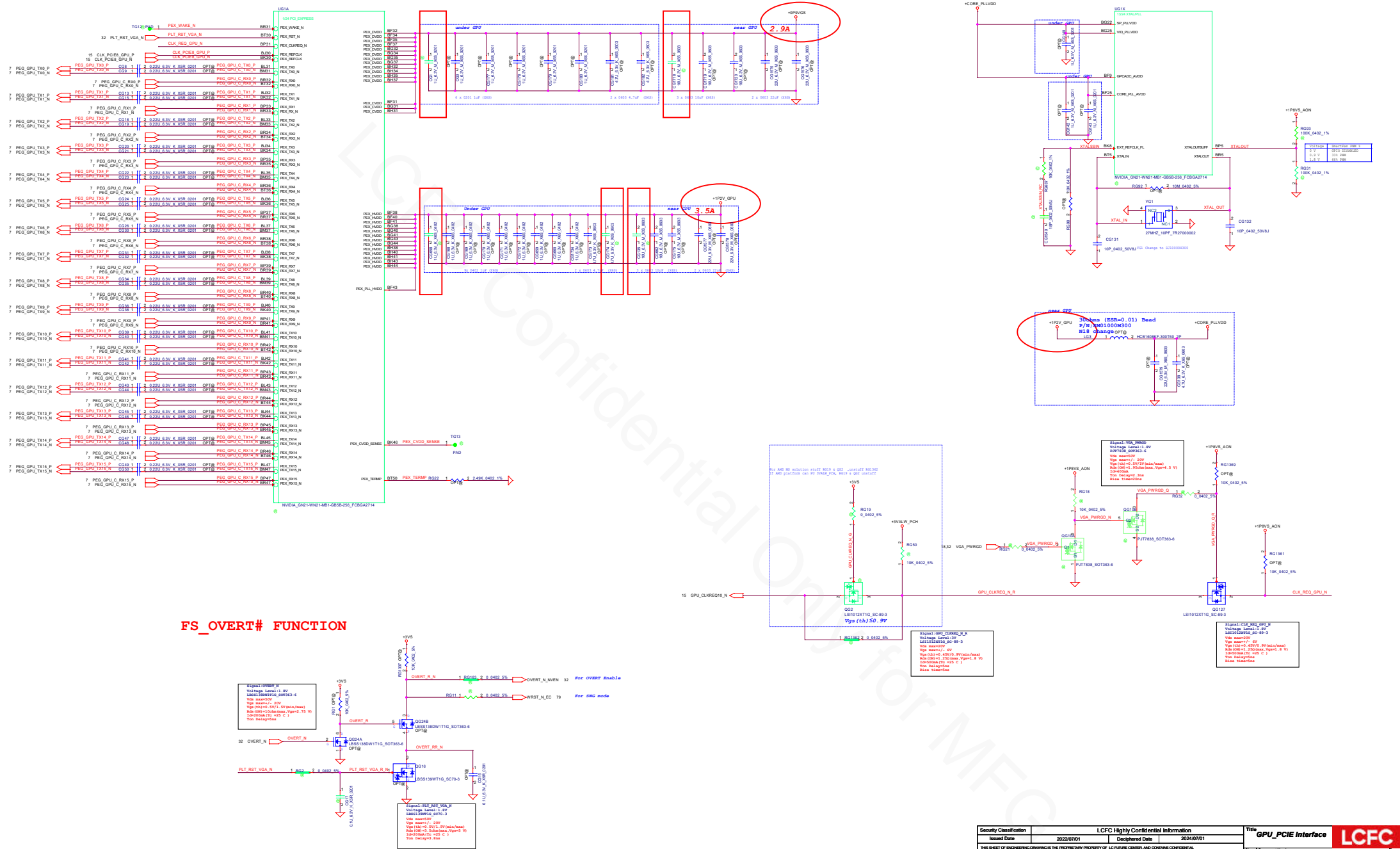




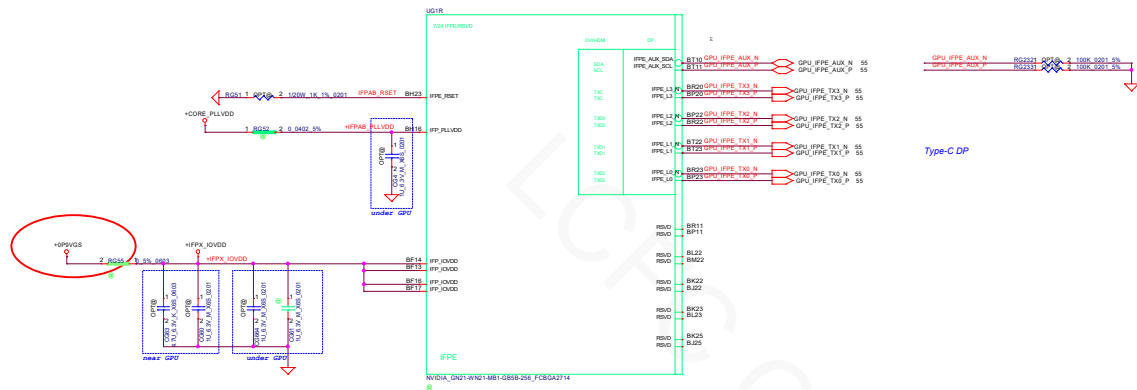


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				Size	Document Number	Rev
					yx0801	0.1
				Date	Wednesday, December 07, 2022	Sheet 20 of 110

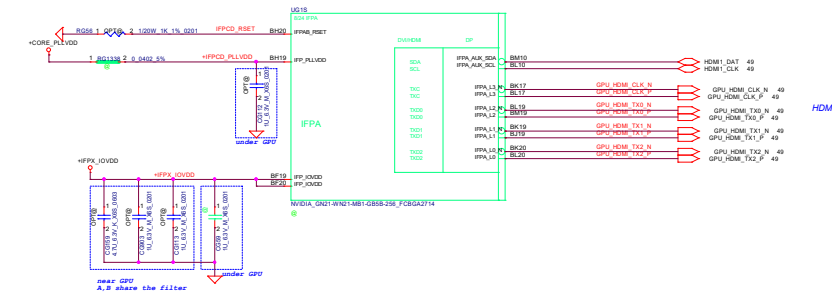




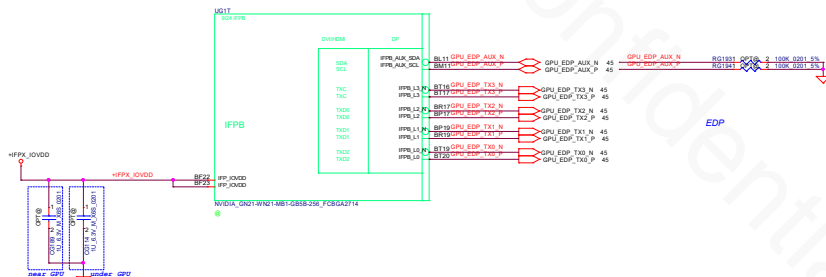
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Revision			1	Document Number	YX801Intel	
Date			2023, November 21, 2023	Sheet	29	of 110



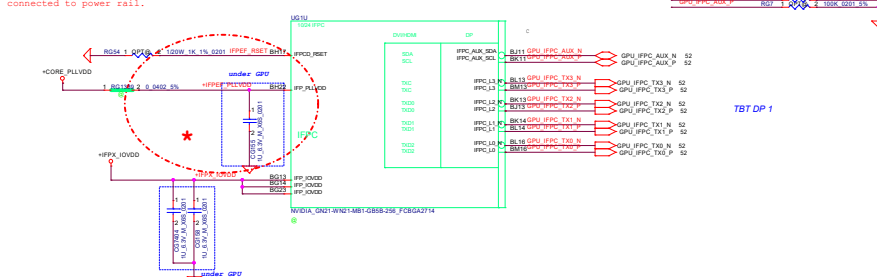
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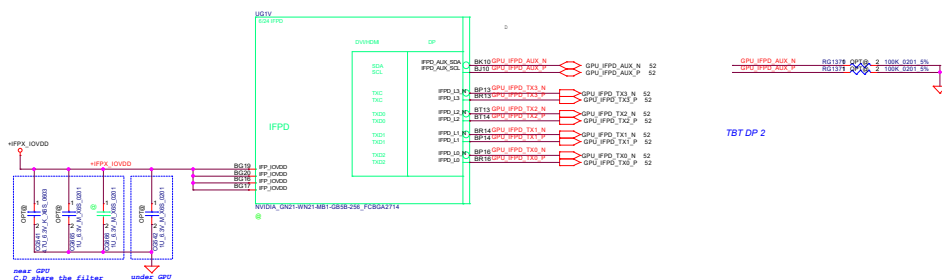
HDMI



EDP



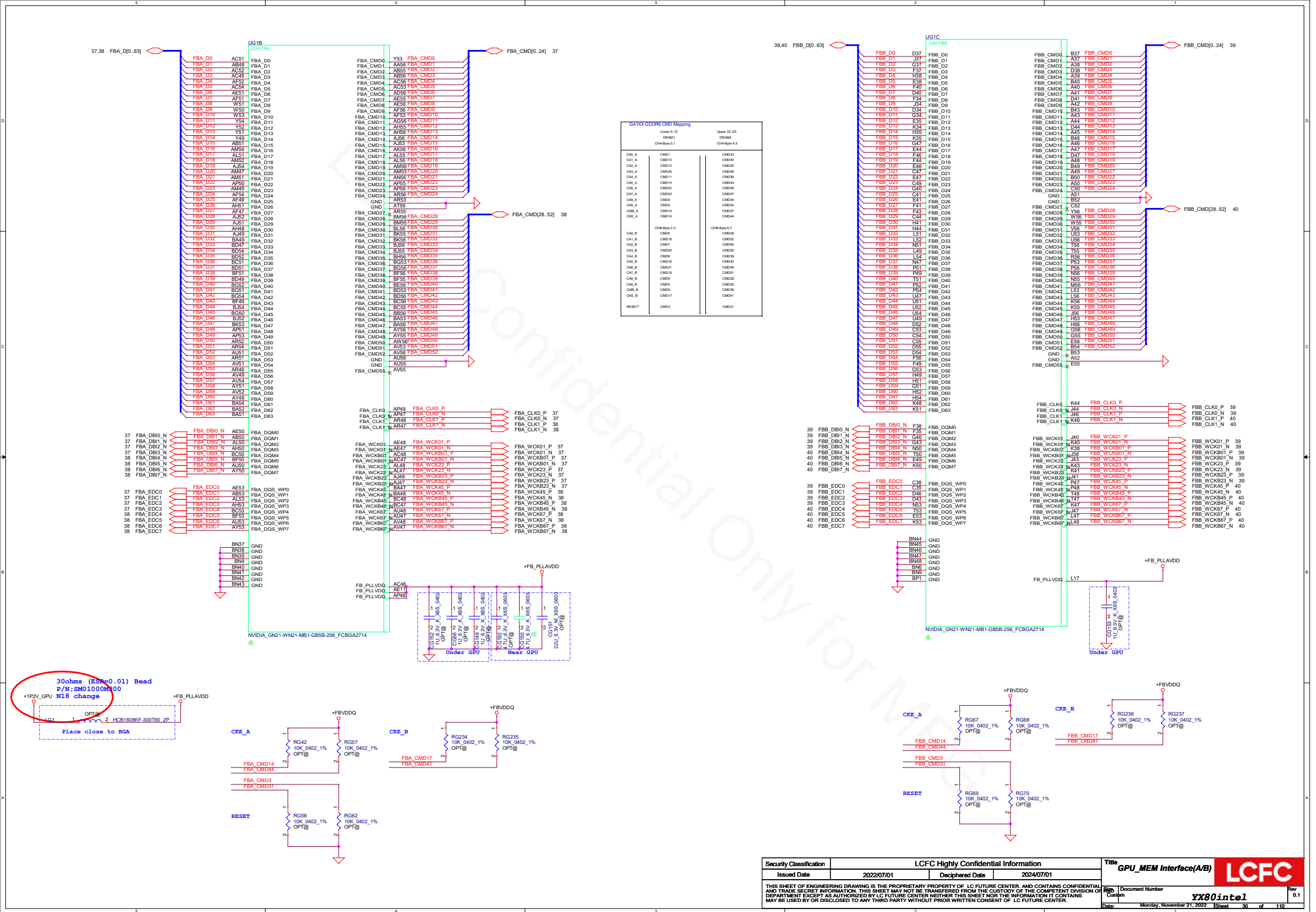
TBT DP 1

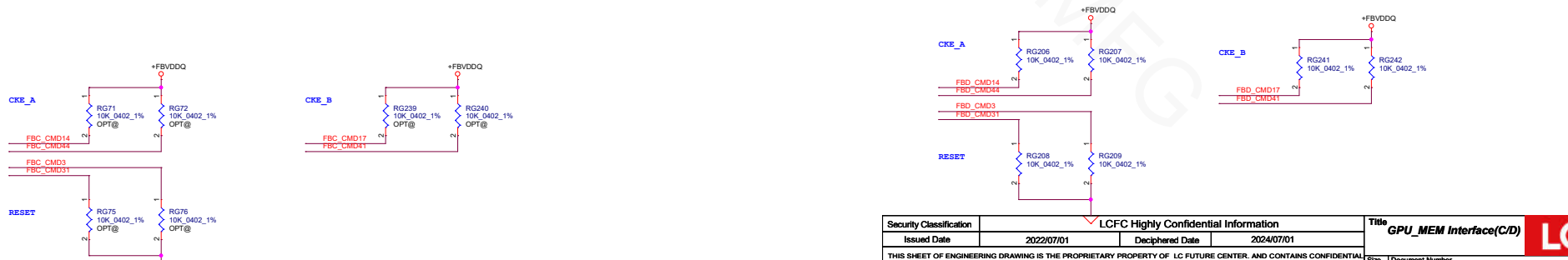



TBT DP 2

For GN20
1. If an IFP link is unused, The main and AUX links, IFPxy_RSET can be left unconnected, and IFPxy_PLLVDD should be 10K PD to GND.
2. IFP_I0VDD rail can be left unconnected if no IFP link is used. If any IFP is used, all IFP_I0VDD balls must be connected to power rail.

For GN21
1. If an IFP link is unused, in general it should be left unconnected. This includes Main and Aux links. IFPxy_RSET (xy = AB, CD, E) can be left unconnected and IFP_PLLVDD should be 10K pull-down to GND if none of IFP is in use. If one of the IFP is used (meaning an IFPxy_PLLVDD ball is connected) then all IFP_PLLVDD die Dumps needs to have power applied.
2. IFP_I0VDD rail can be left unconnected if no IFP link is used. If any IFP is used, all IFP_I0VDD balls must be connected to power rail.





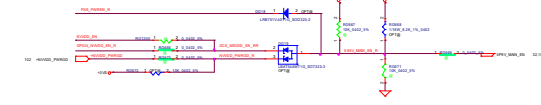
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Power on/off sequence

NVDD_EN



0.90V_MA1N_EN



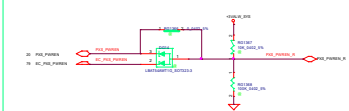
FWDDQ_PWR_EN



VGA_PWDQ

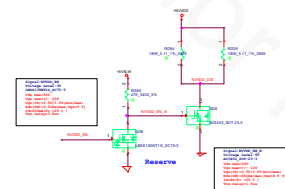


NOTES:
For A60 platform support, 上电0514/051365, 不上电051365, 平台唤醒pull up

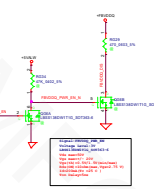


Discharge

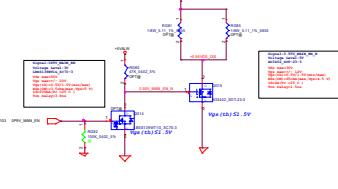
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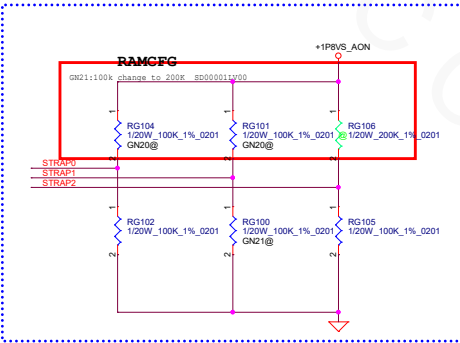
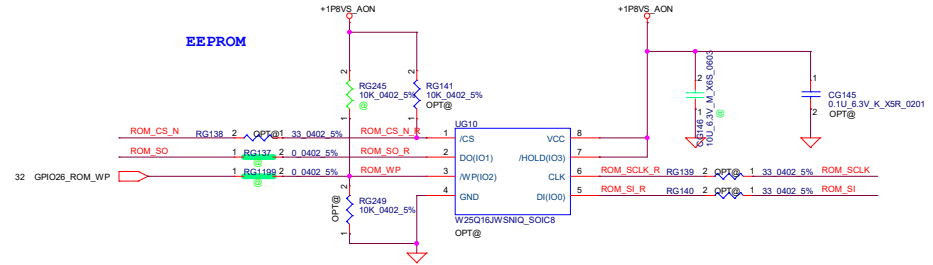
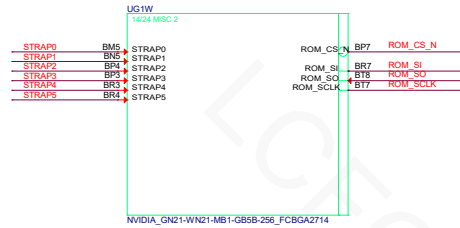


FWDDQ Discharge



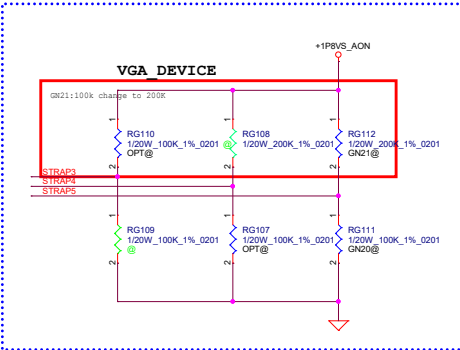
+0.9VGS Discharge





MB1	RAMCFG[2:0]	STRAP2	STRAP1	STRAP0
K42AF325BC-SC20	0 (0x0000)	L	L	L
K42AF325BC-SC20 (GN20E)	11 (0x000B)	L	H	M

MB2	RAMCFG[2:0]	STRAP2	STRAP1	STRAP0
K42AF325BC-SC16	10 (0x000A)	L	M	H
H56G42AS4DX014	8 (0x0008)	L	L	M



VGA_DEVICE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
H	L	H	0	1	0	1

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

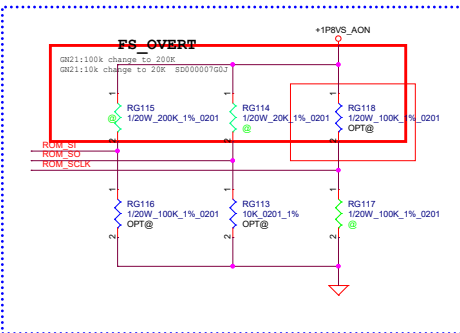
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

VGA_DEVICE (GN20E)

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	H	0	0	0	1

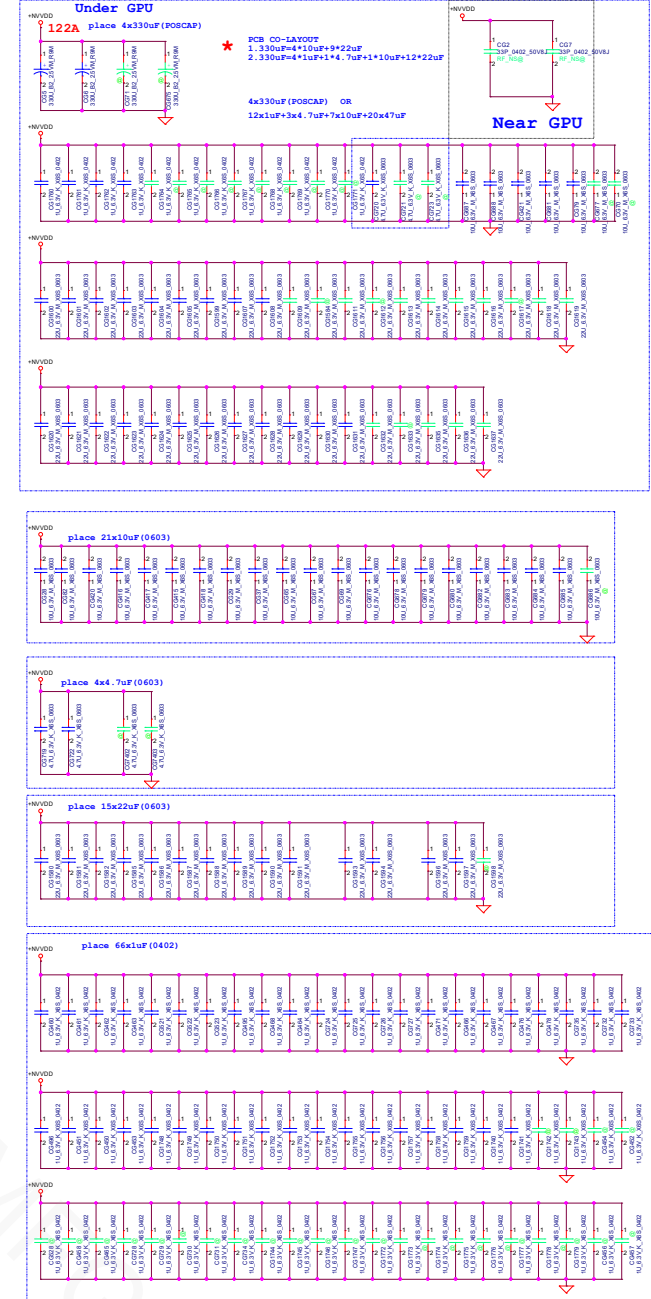
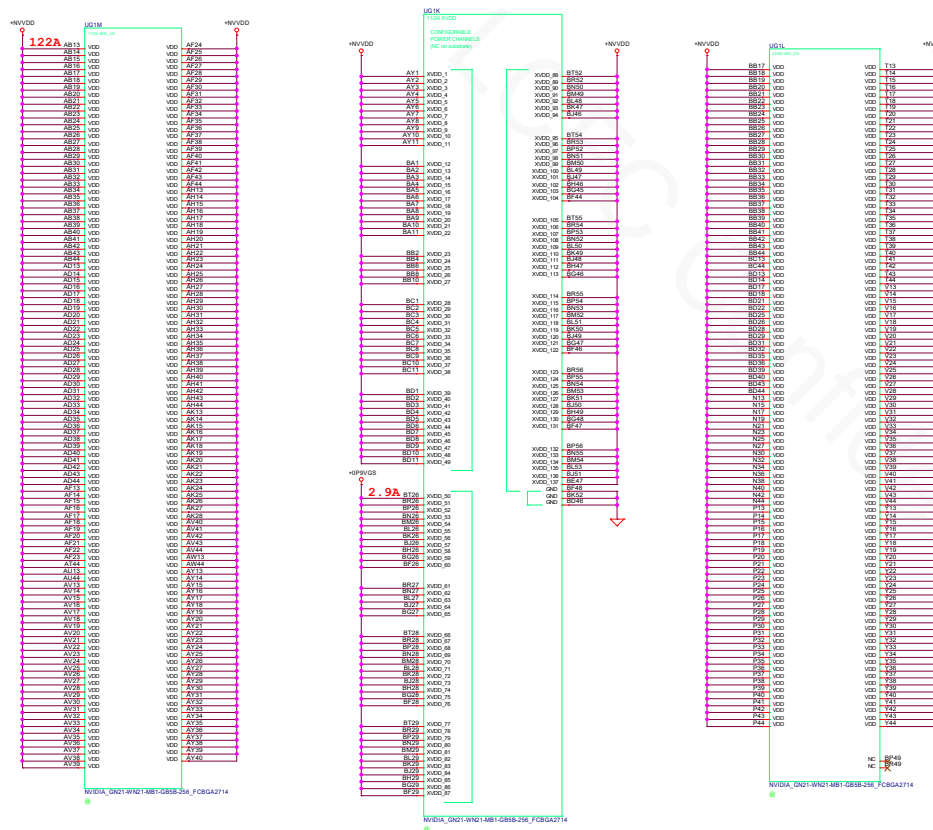


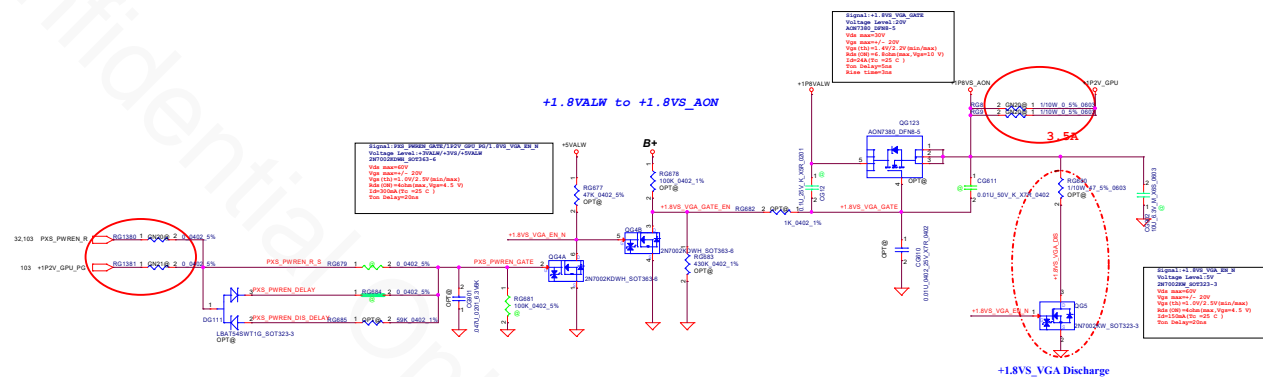
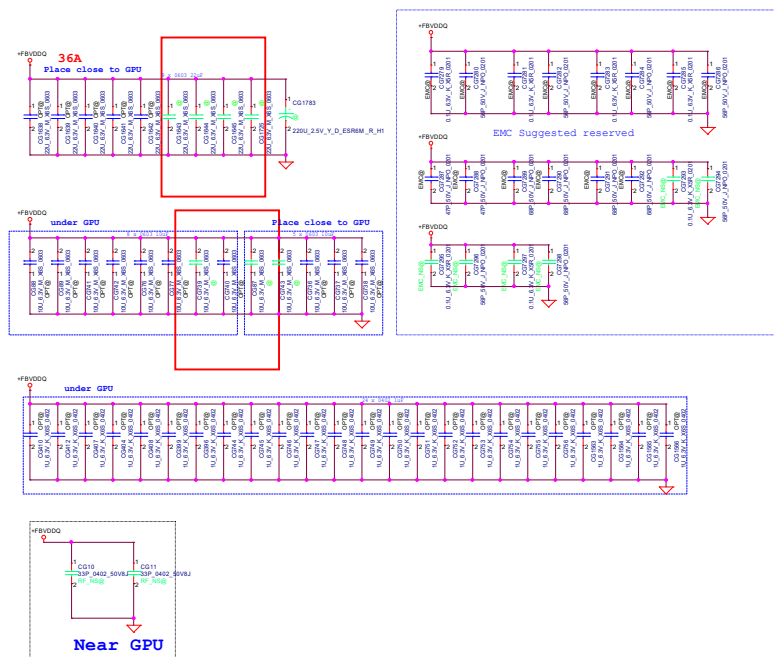
FS_OVERT

GPU	ROM_SO	ROM_SI	ROM_SCLK	FS_OVERT
GN20x	L	L	L	DISABLE
GN20x	L	L	H	ENABLE (default)

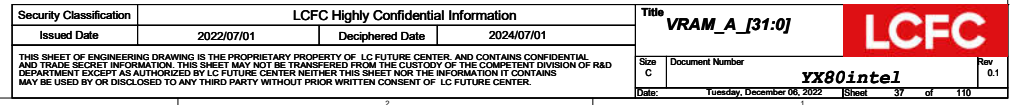
FS_OVERT

GPU	ROM_SO	ROM_SI	ROM_SCLK	FS_OVERT
GN21x	L	L	L	DISABLE
GN21x	L	L	H	ENABLE (default)

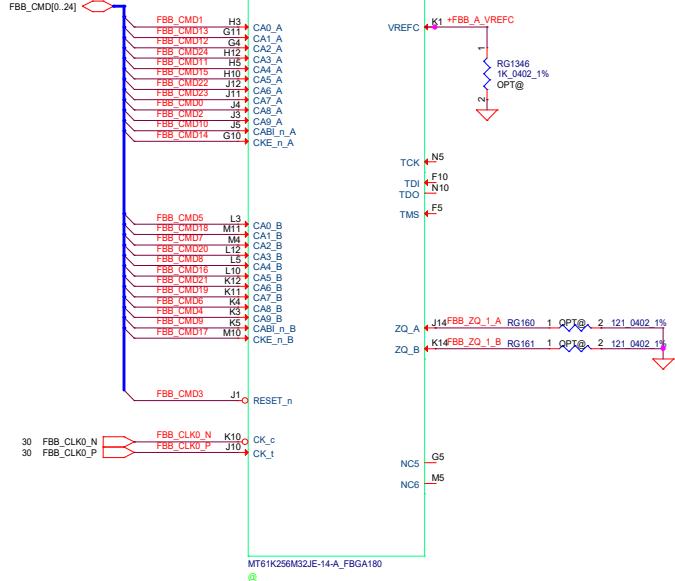
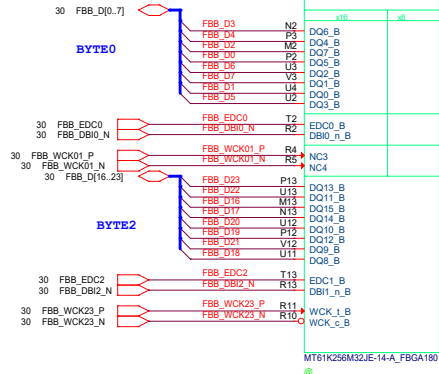
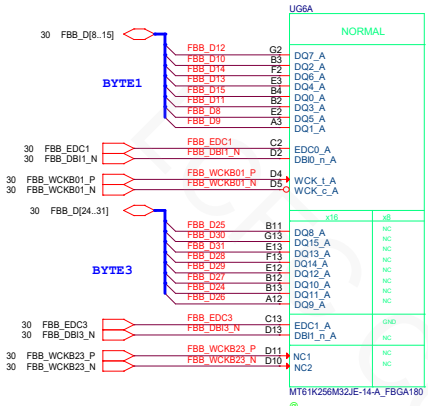
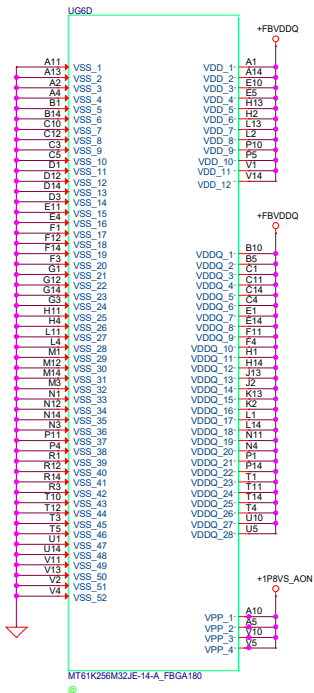




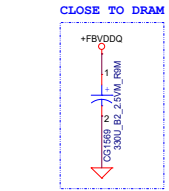
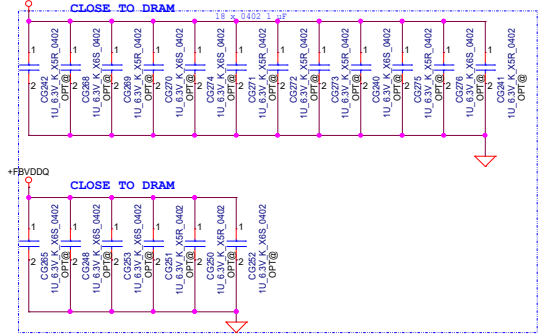
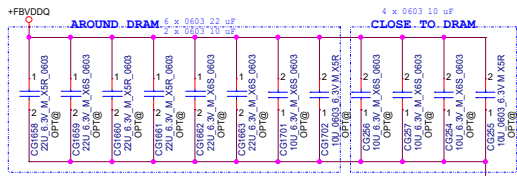
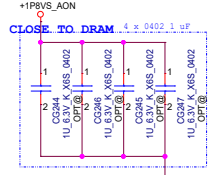
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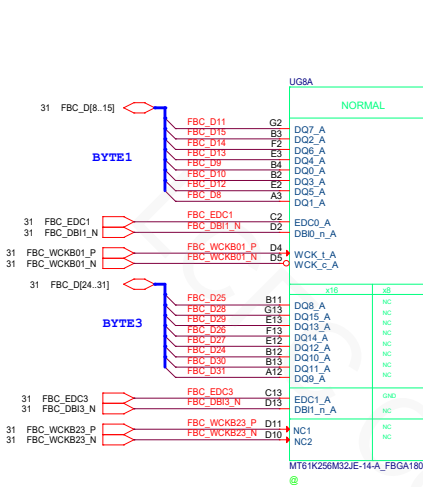
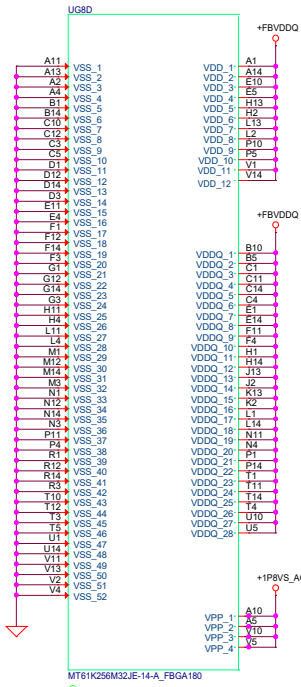




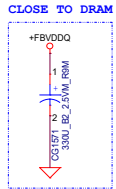
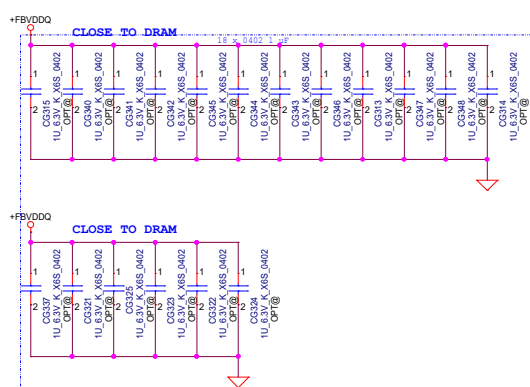
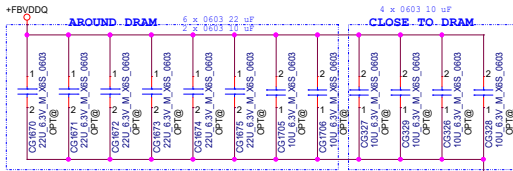
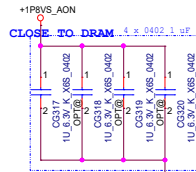
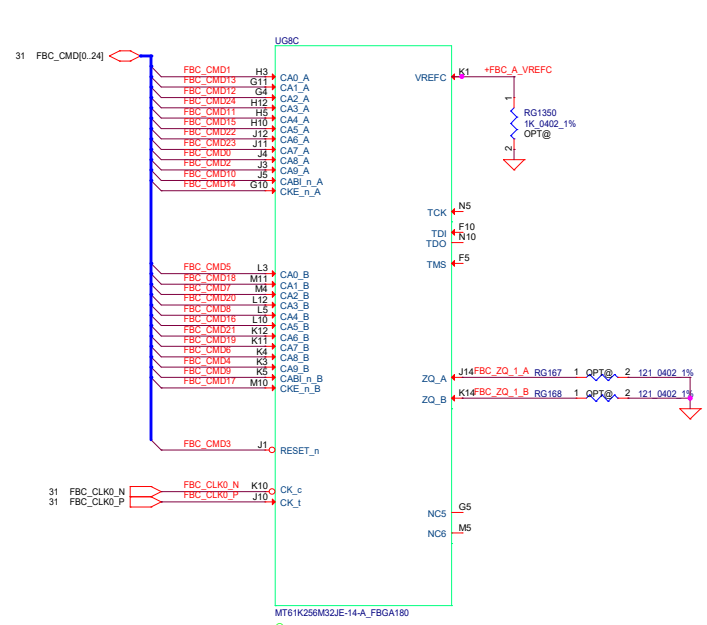
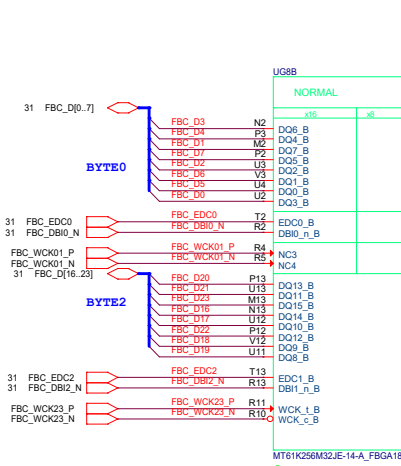


follow CRB bit swap

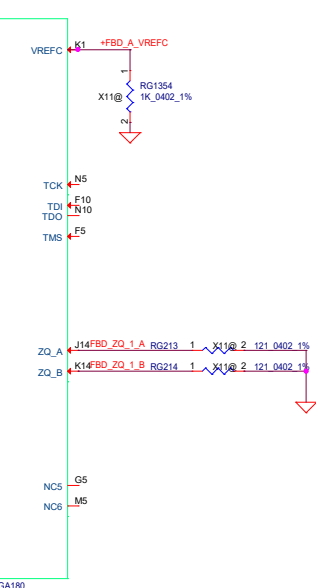
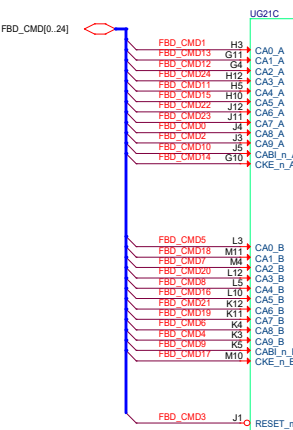
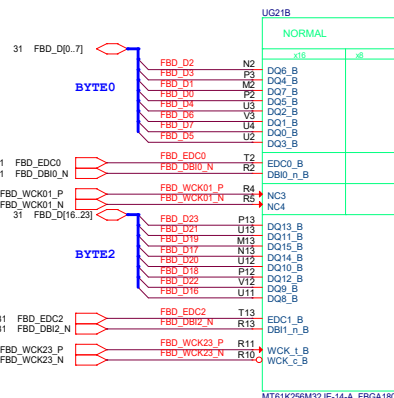
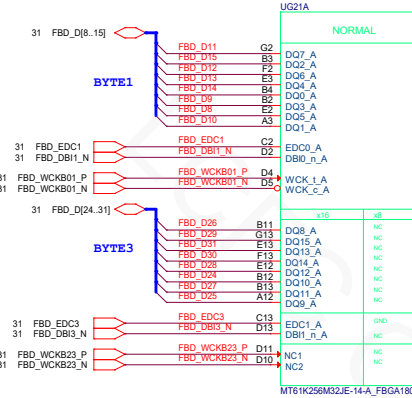
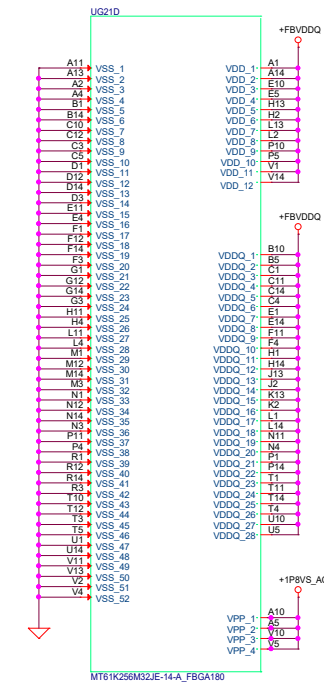




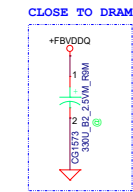
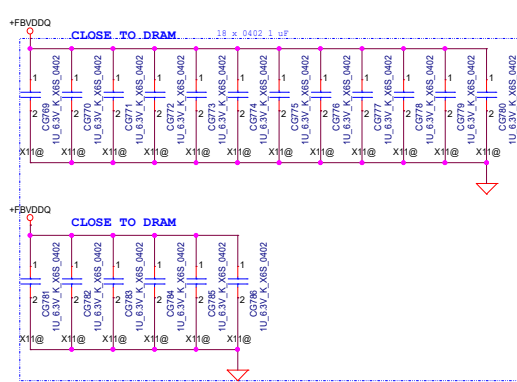
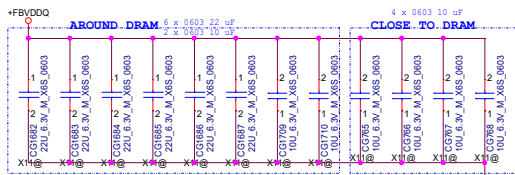
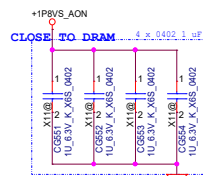
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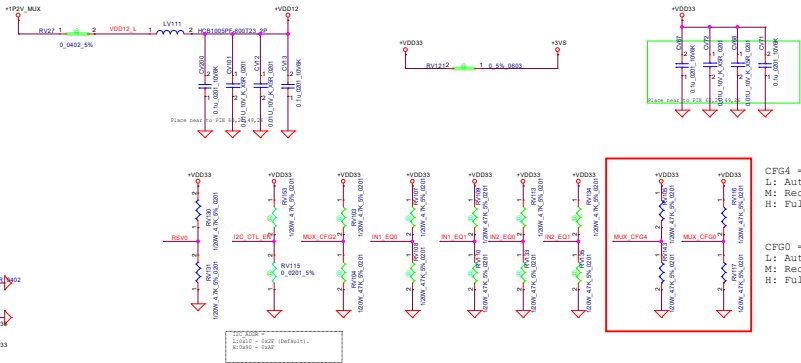
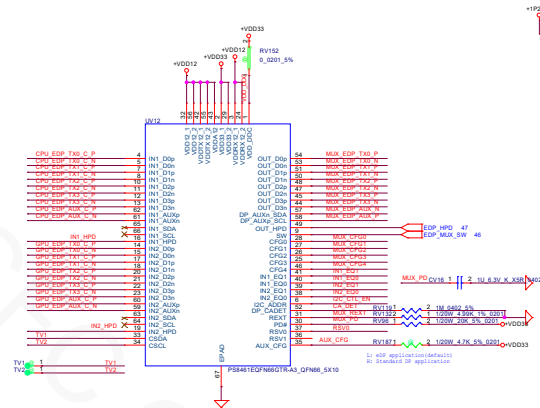
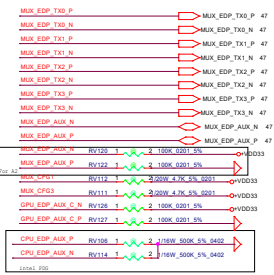
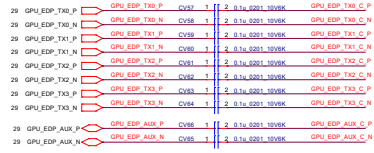
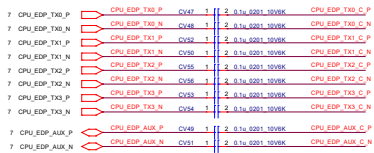


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Size		Document Number				Rev
		YX80intel				0.1
Date:		Monday, August 08, 2022		Sheet		42 of 110



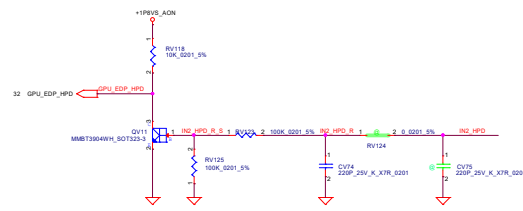
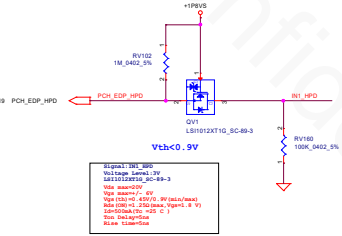
follow CRB bit swap





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M: Redriving mode
H: Full jitter cleaning mode

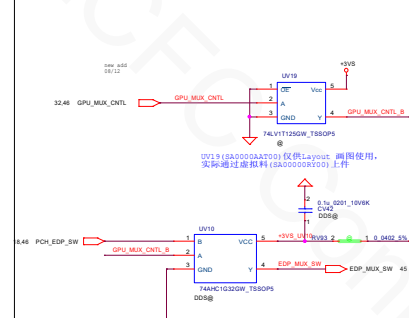
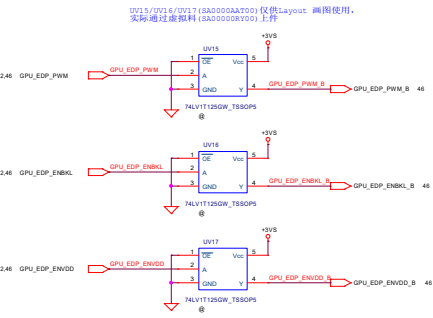
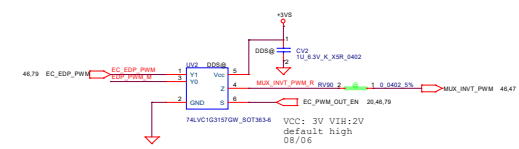
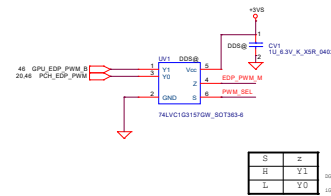
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M: Redriving mode
H: Full jitter cleaning mode



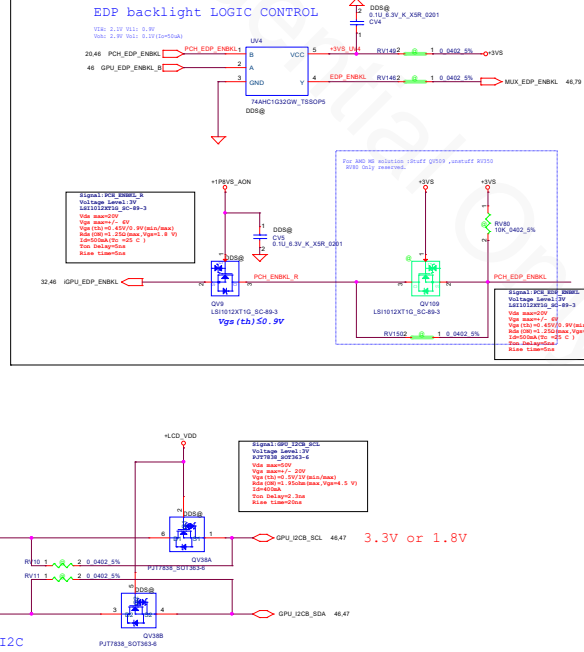
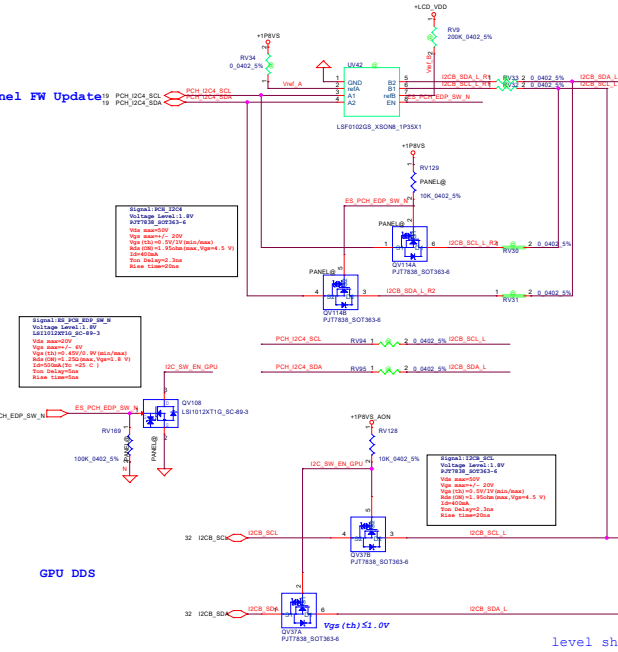
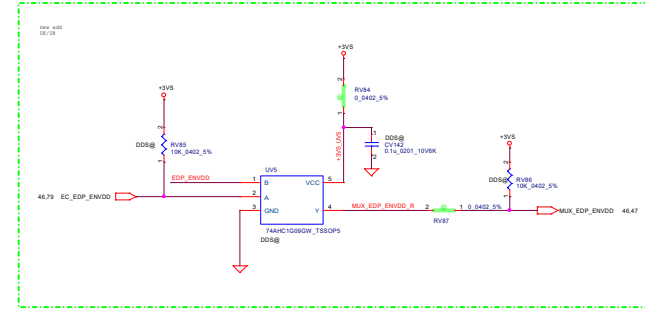
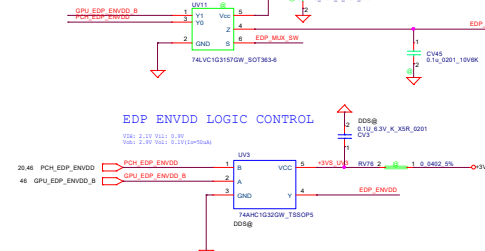
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Doc		YX001intel		Doc		YX001intel		Rev			



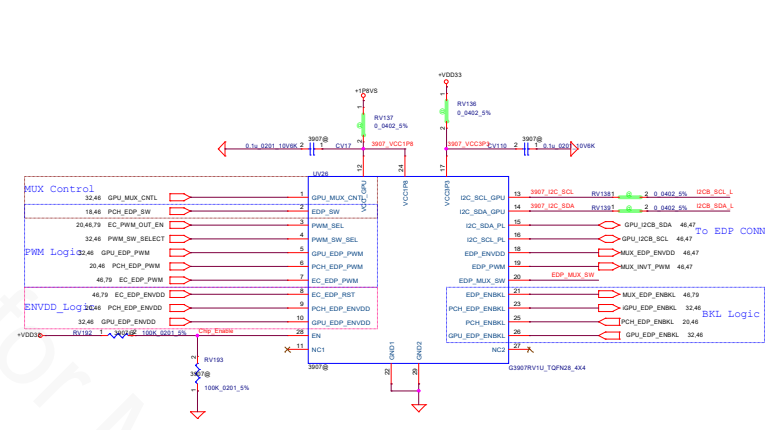
EDP PWM LOGIC CONTROL



Co-lay EDP ENVDD LOGIC CONTROL

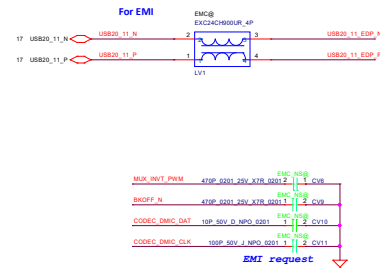
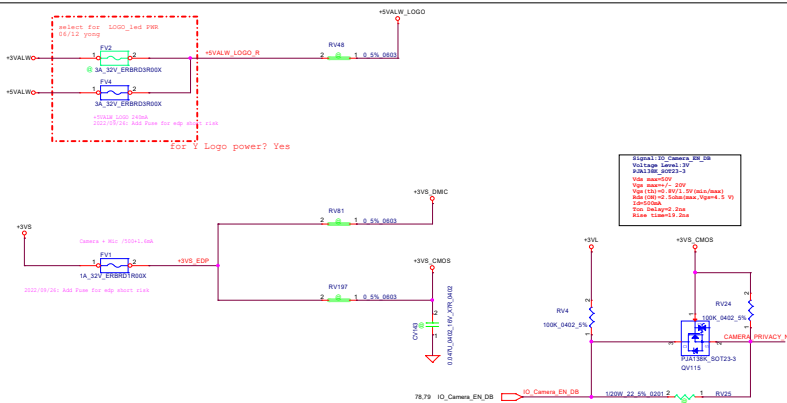
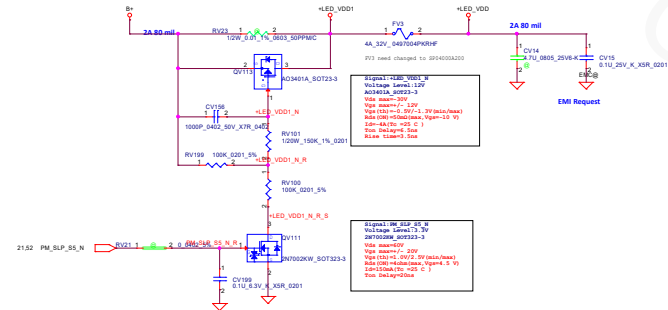
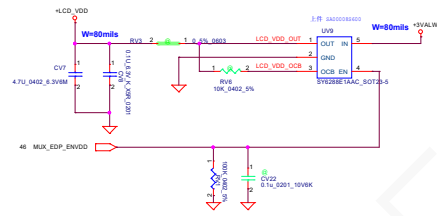


G3907 DDS COLAY

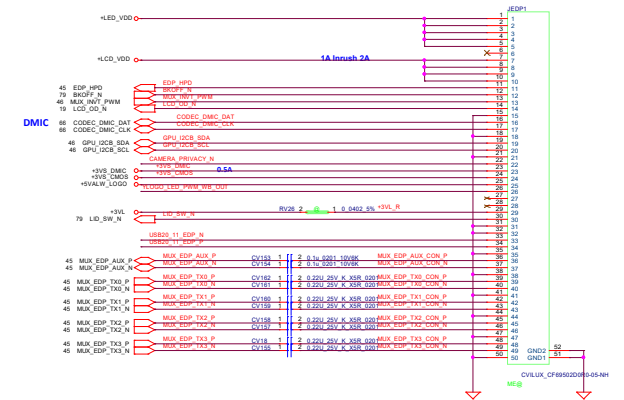
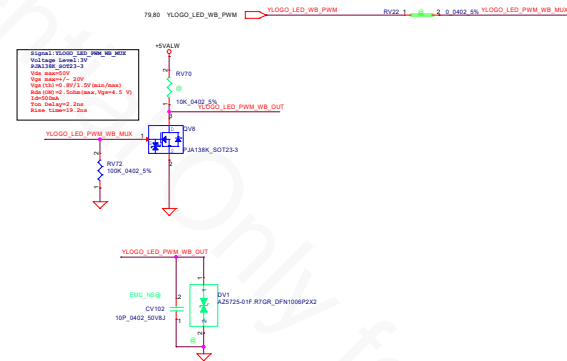


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Issued Date		2023/07/01		NV DDS LOGIC	
Issued Date		2023/07/01		LCFC	
Document Number		YX80101		61	

LCD POWER CIRCUIT



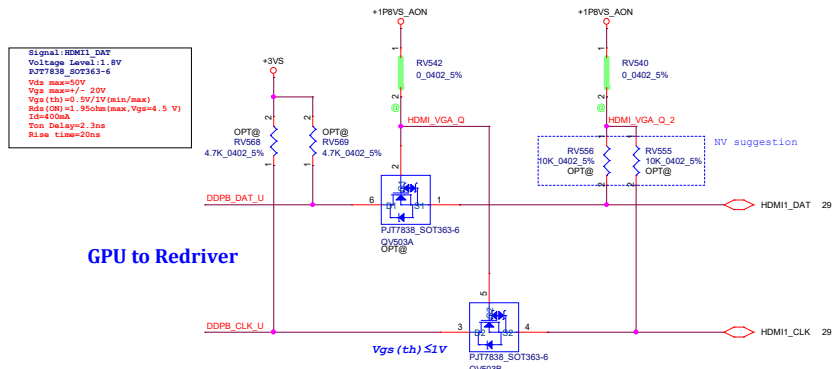
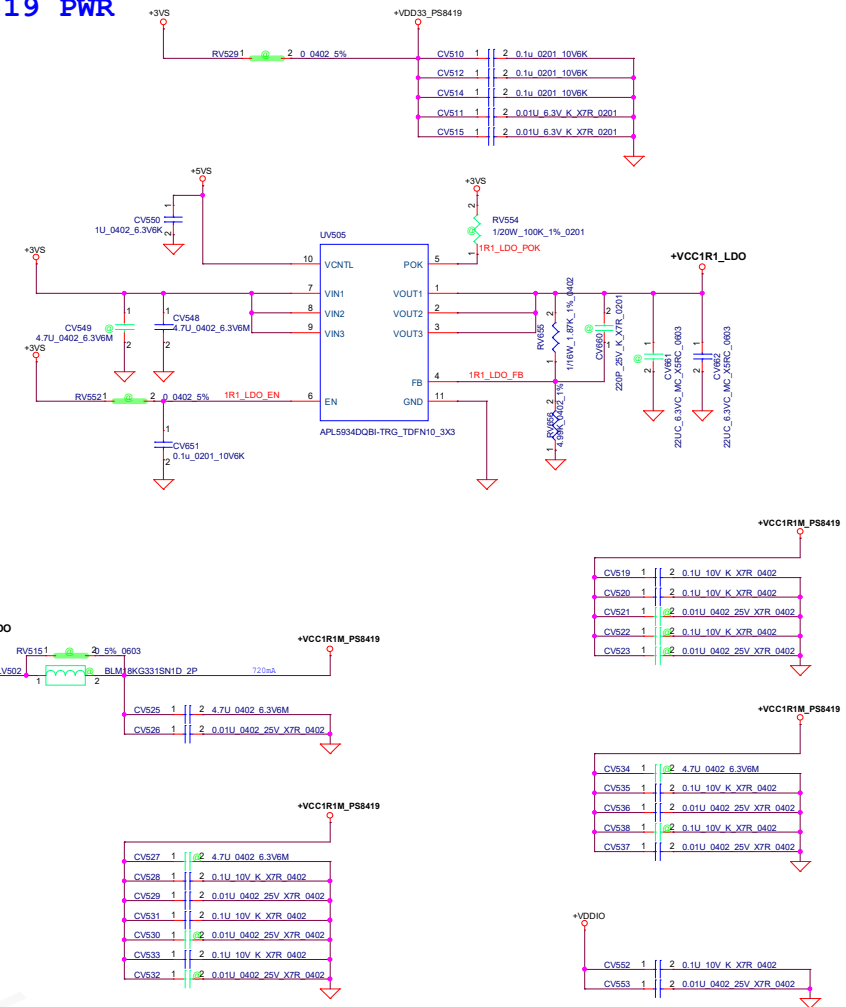
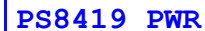
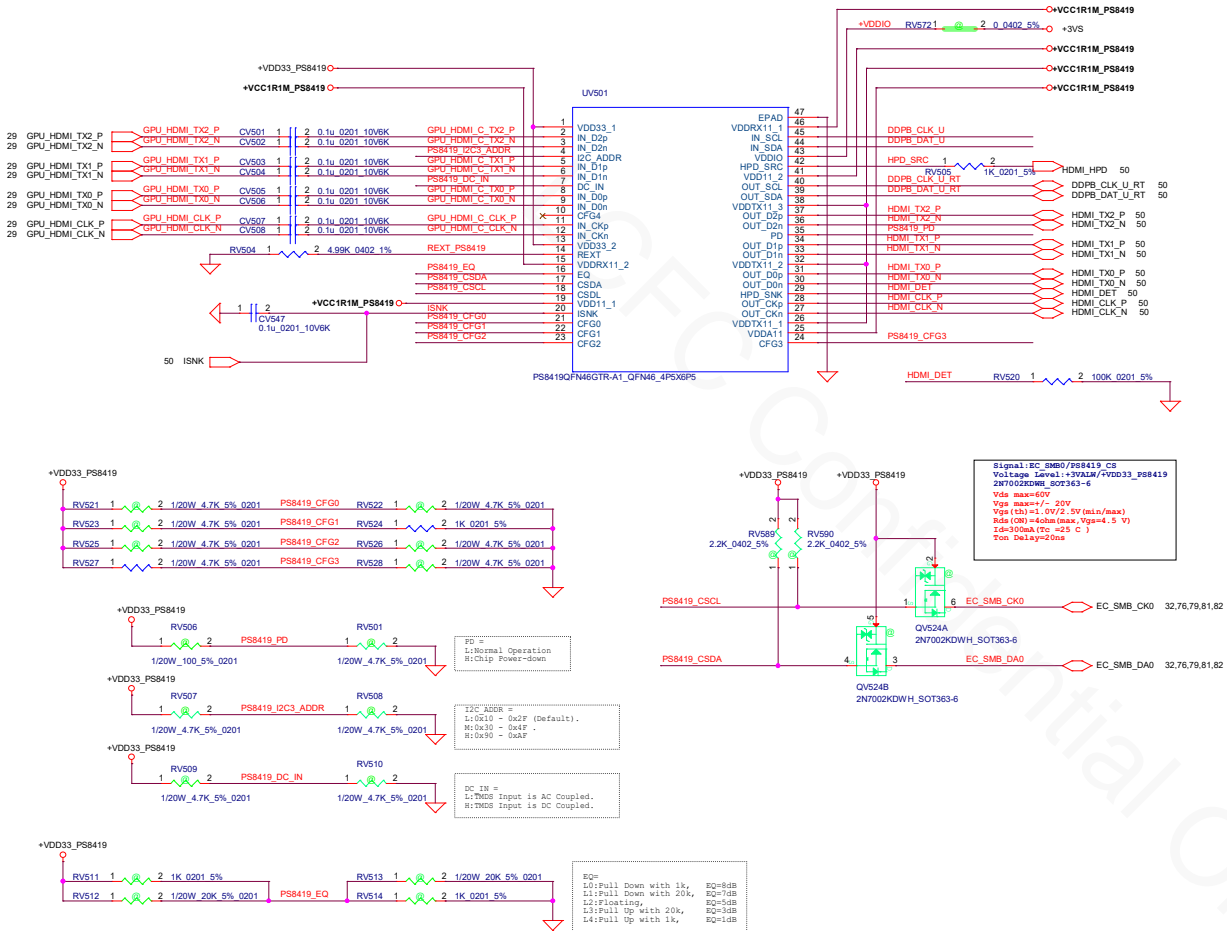
Y LOGO




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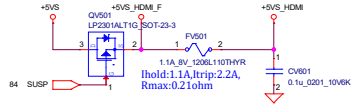
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HDMI2.1 Retimer PS8419

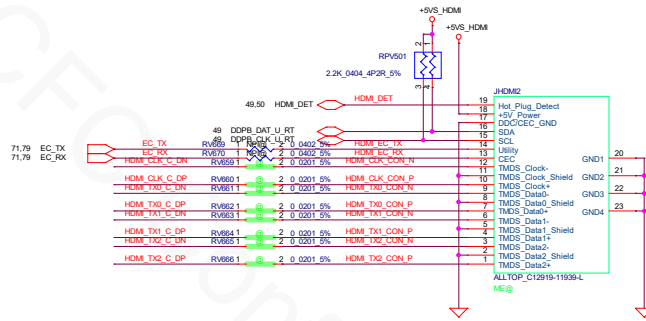
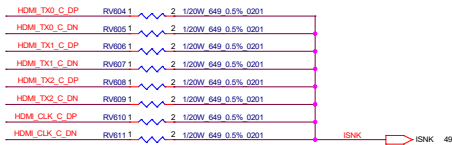
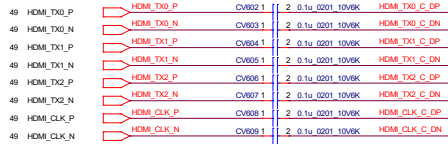


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				Date:	Sunday, December 11, 2022		49 of 110
				Rev	0.1		

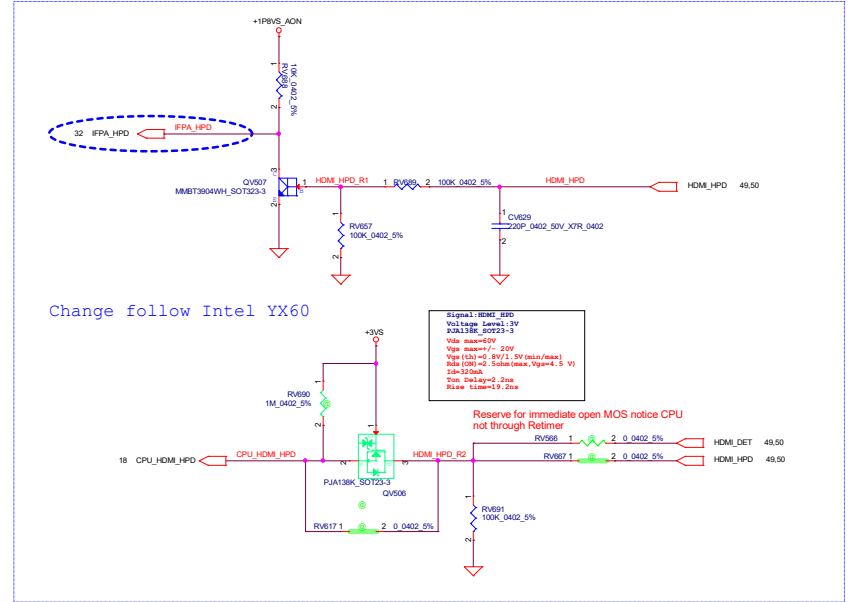
HDMI Power



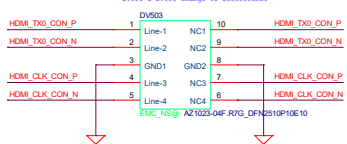
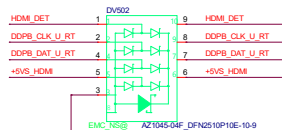
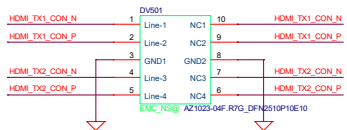
Signal: B0SP
Voltage Level: 1.5V
LP2118A723_001-23-3
Vds max=-20V
Vgs max=+/- 5V
Vgs(th)=0.4V/-1V(min/max)
Rds(on)=0.002ohm(max, Vgs=2.5 V)
Idd=2A(Ps=25 C)
Ton Delay=50us
Rise time=30us



Change follow Intel YX60



EMC

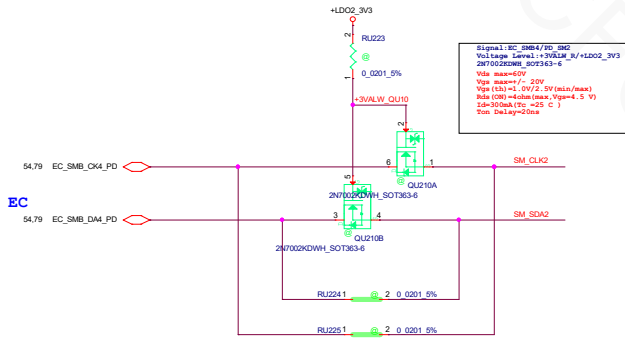


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Custm		YX80intel		0.1							
Date		Monday, November 28, 2022		Sheet		80		of		110	

Ra

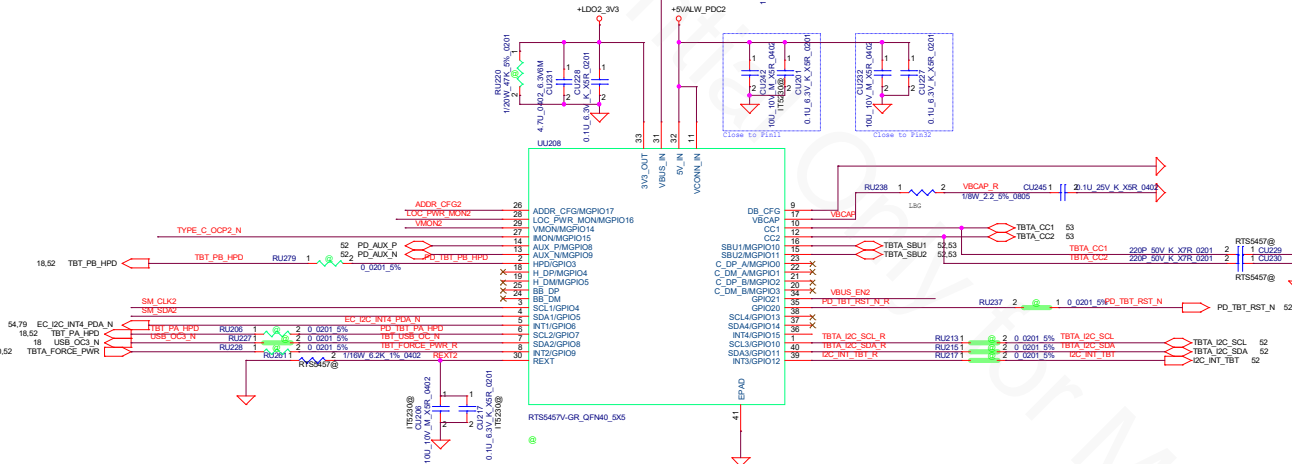
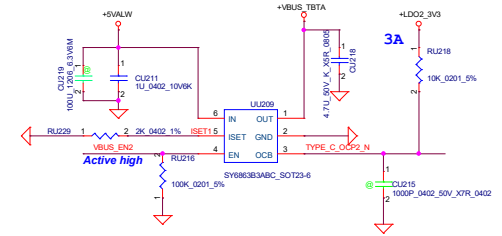
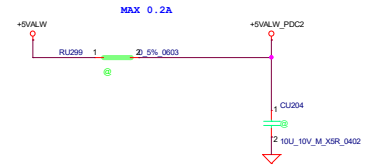
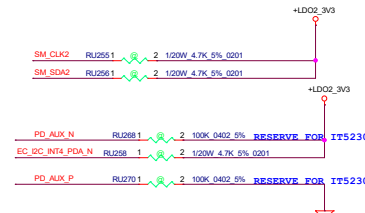
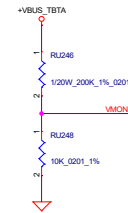
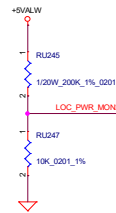
Rb

Slave Addr	Ra	Rb	
addr0 : 0xCC	NC	10K	< 0.2 V
addr1 : 0xCE	75K	10K	$\geq 0.2 \text{ V} \ \&\& \ < 0.6 \text{ V}$
addr2 : 0xD0	33K	10K	$\geq 0.6 \text{ V} \ \&\& \ < 1.0 \text{ V}$
addr3 : 0xD2	10K	10K	$\geq 1.0 \text{ V}$

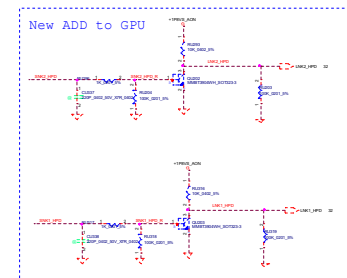
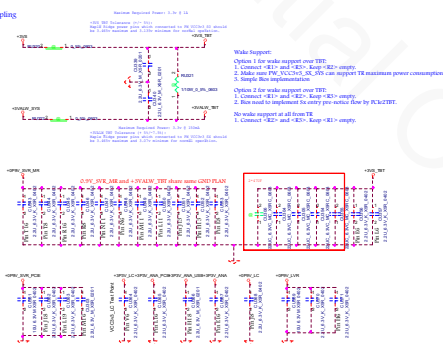
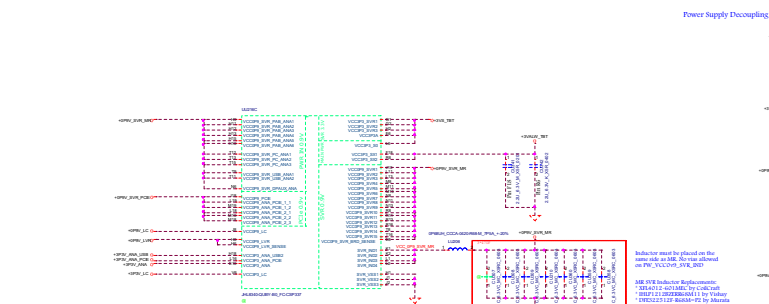
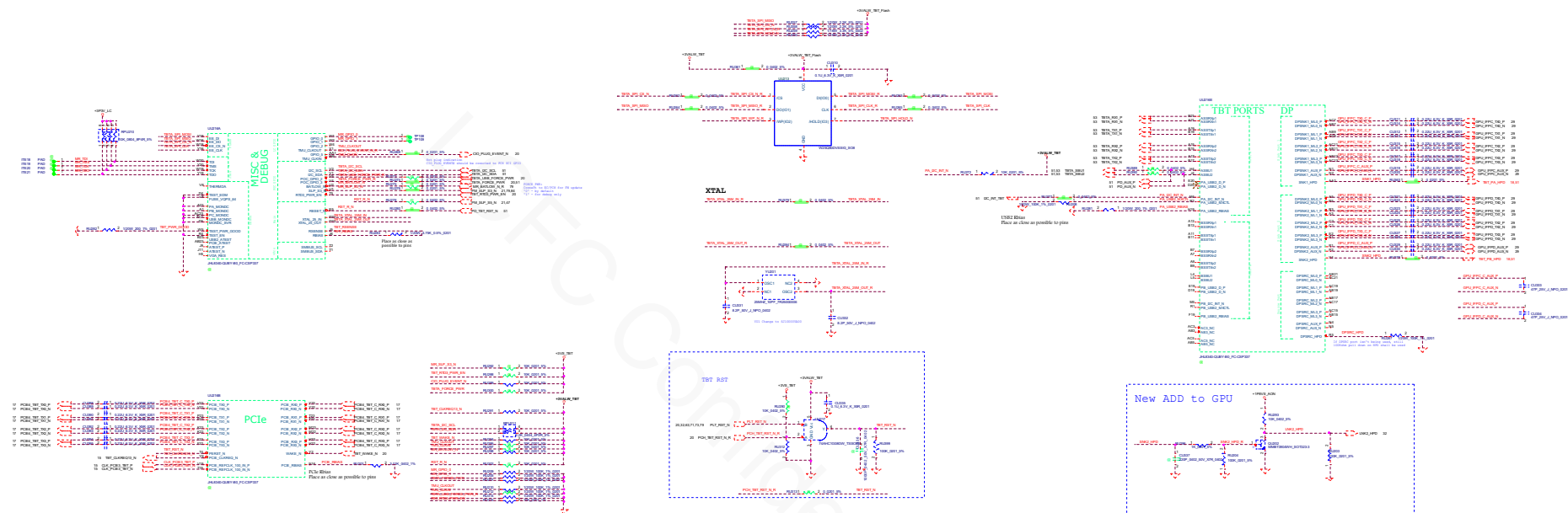


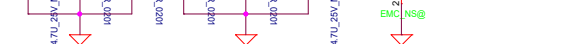
Signal: EC_SMB4/S0_SMC
Voltage Level: +5VALW_N/+5VALW_P/+LDO2_3V3
247002DWH_SOT363-6

Vda max=4.0V
Vga max=1.0V
Vga (th)=1.0V/2.5V(min/max)
Rda (DR)=4.0k(max)/Vga=4.5V
Idd=300mA (To >25 C)
Rda Delay=0.5ms

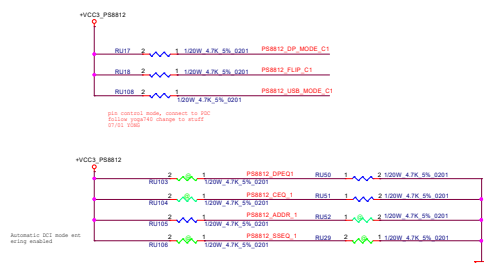
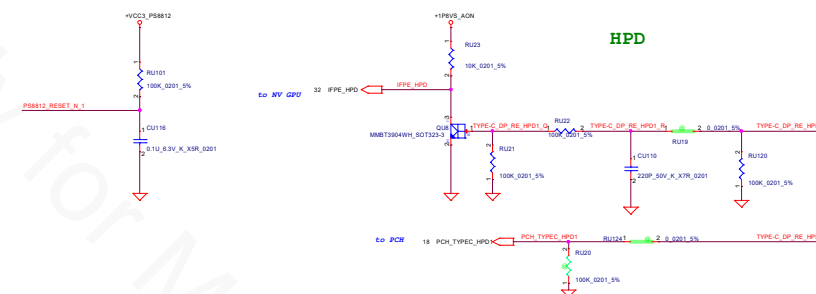
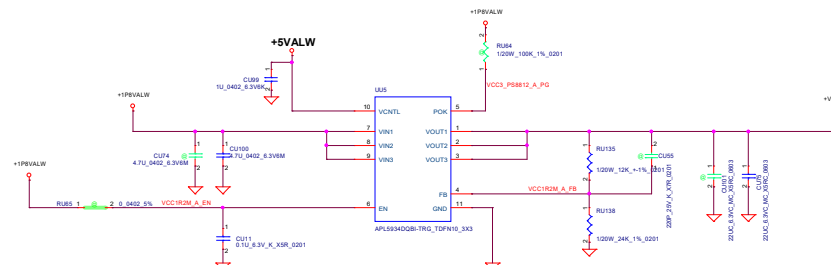
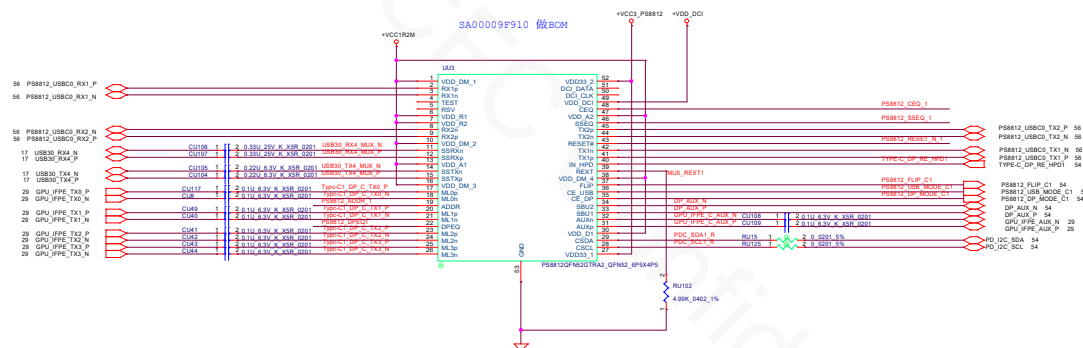
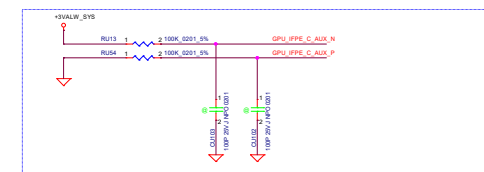
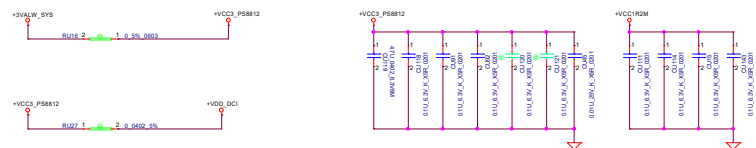


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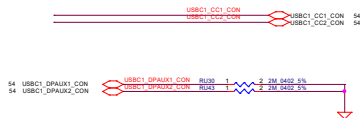


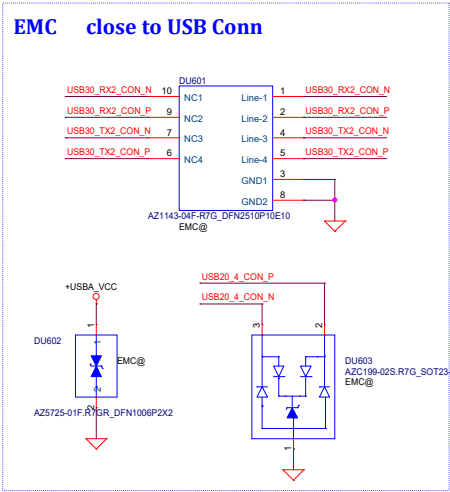
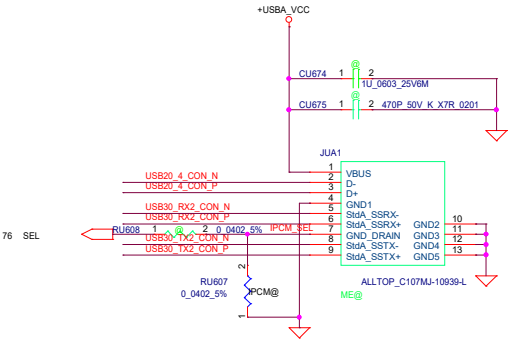
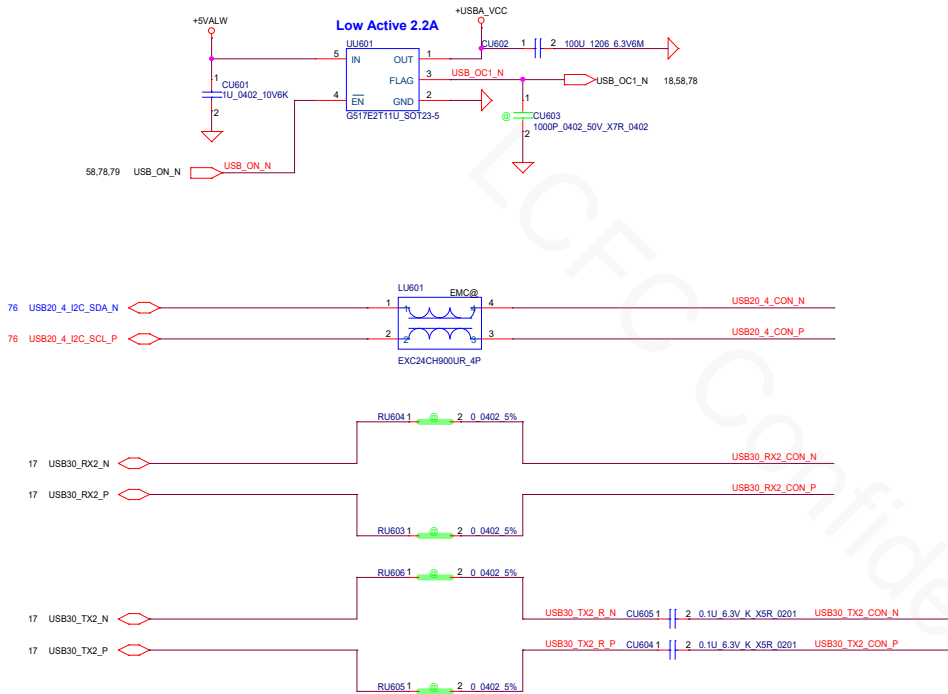


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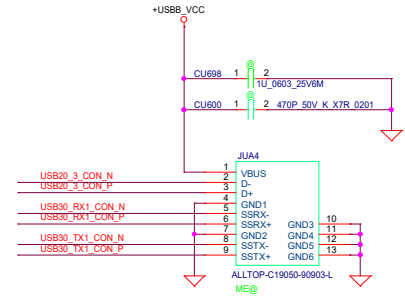
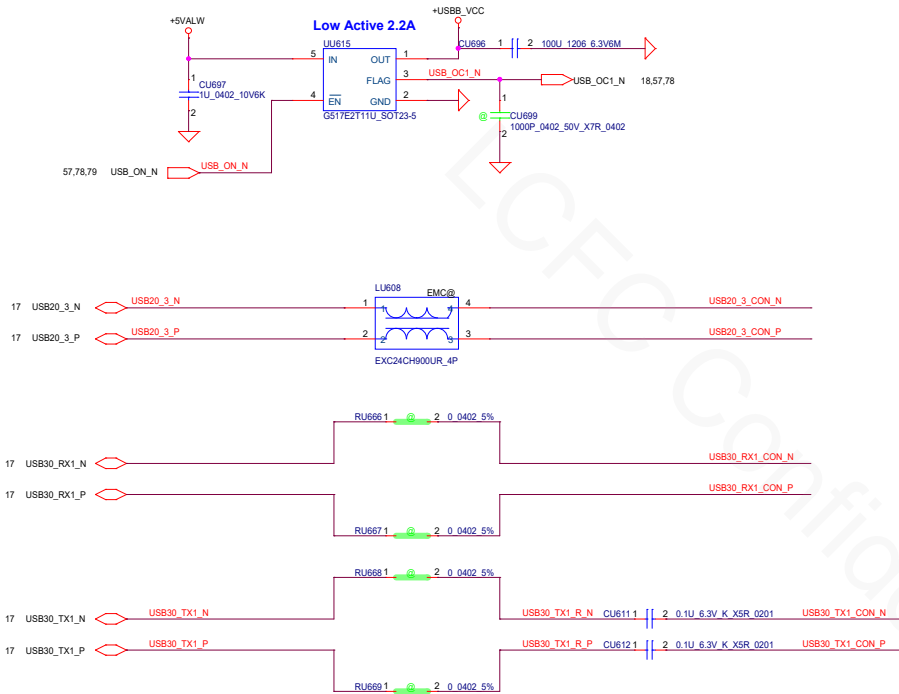


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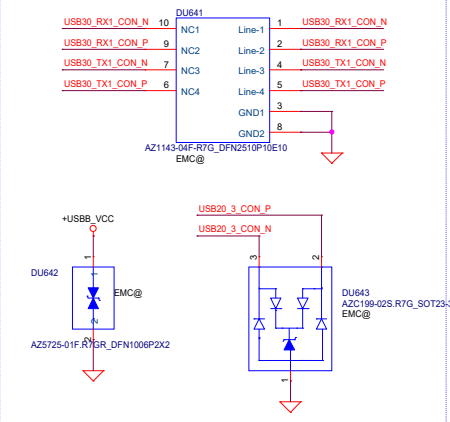




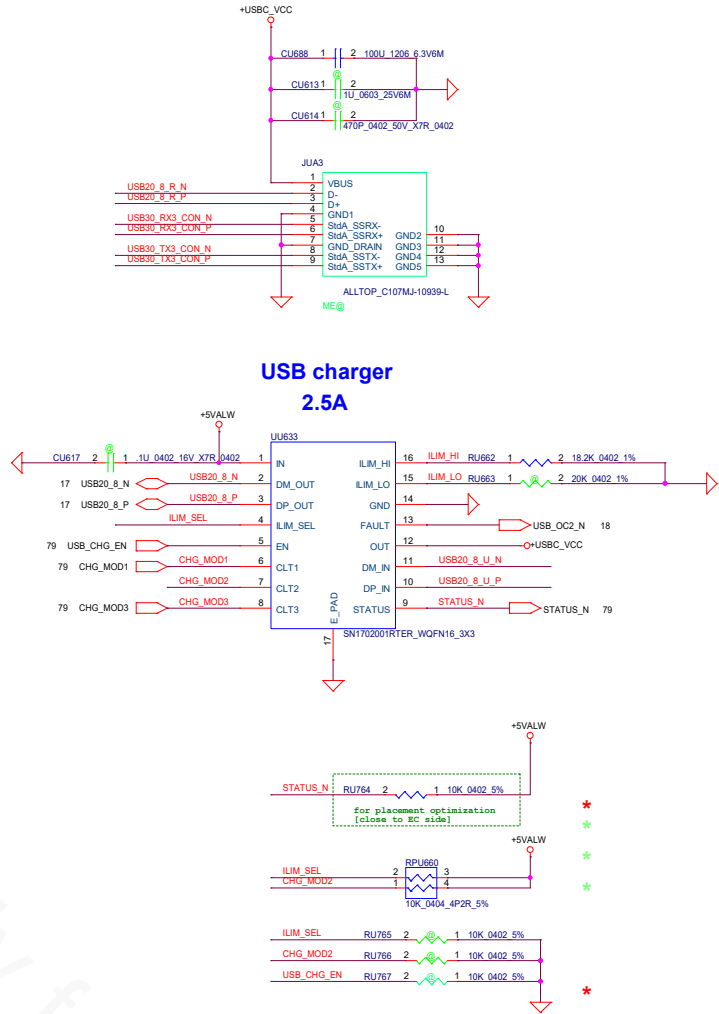
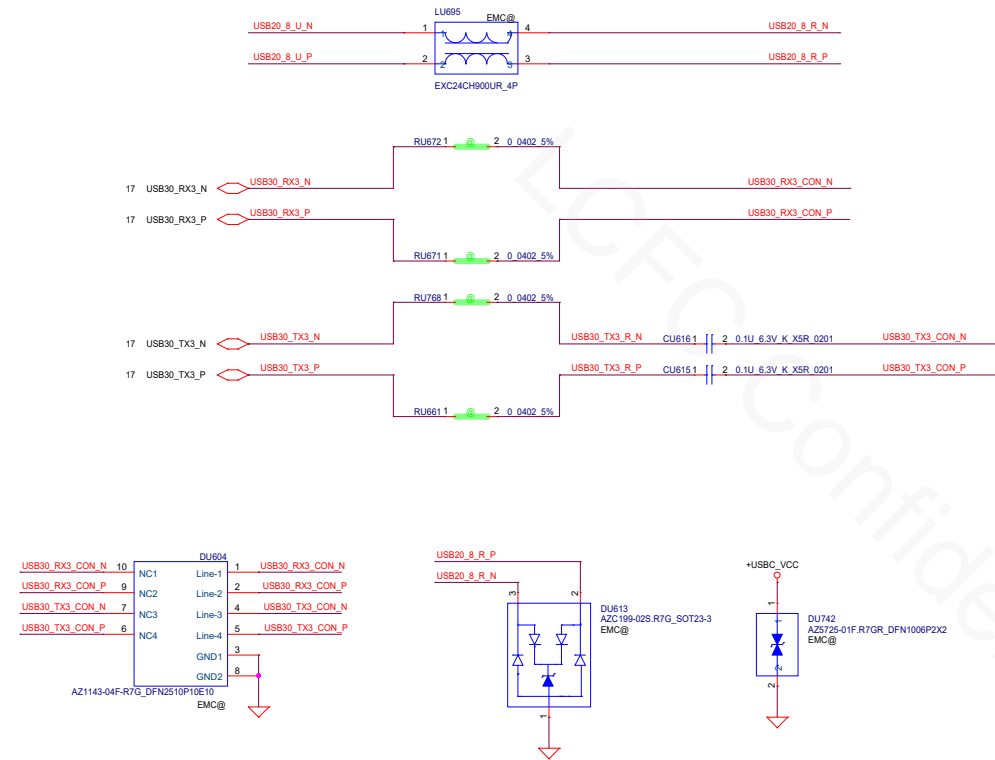
LEFT USBA



EMC close to USB Conn




BACK USBA AOU



CLT1	CLT2	CLT3	ILIM_SEL	MOD
0	0	0	X	DCB OUT held low
1	1	1	1	CDP Data Connected and Port Power Mgt. Function Active
1	1	1	0	SDP2 Data Connected
1	1	0	X	SDP1 Data Connected
0	1	0	X	SDP1 Data Connected
1	0	0	X	DCP_Short Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	DCP_Auto Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto Data Disconnected and Power Wake Function Active

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Unit						0.1
Date	Monday, August 08, 2022		Sheet	80	of	110

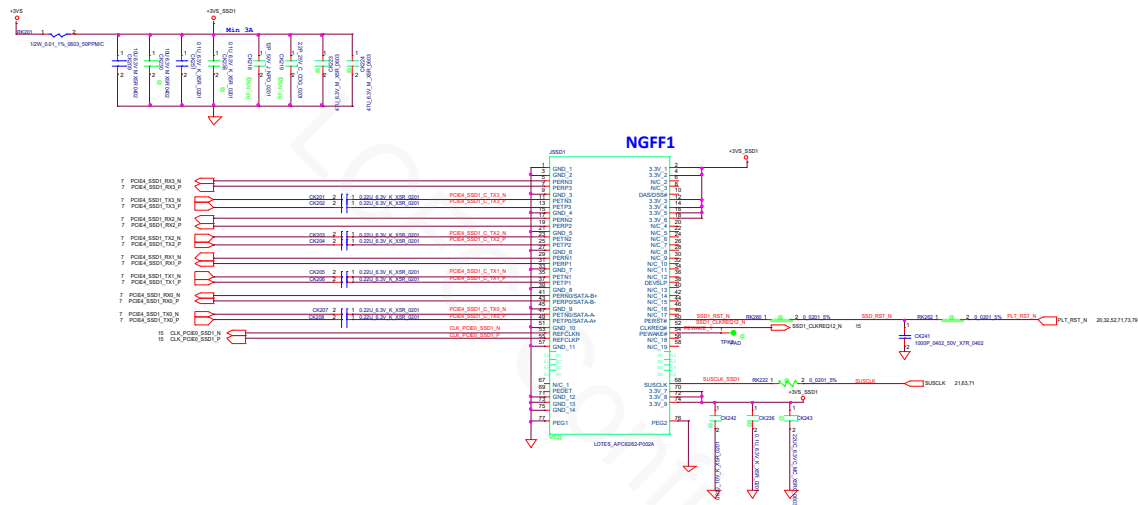
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<small>Issue: 10/20/2023</small>					

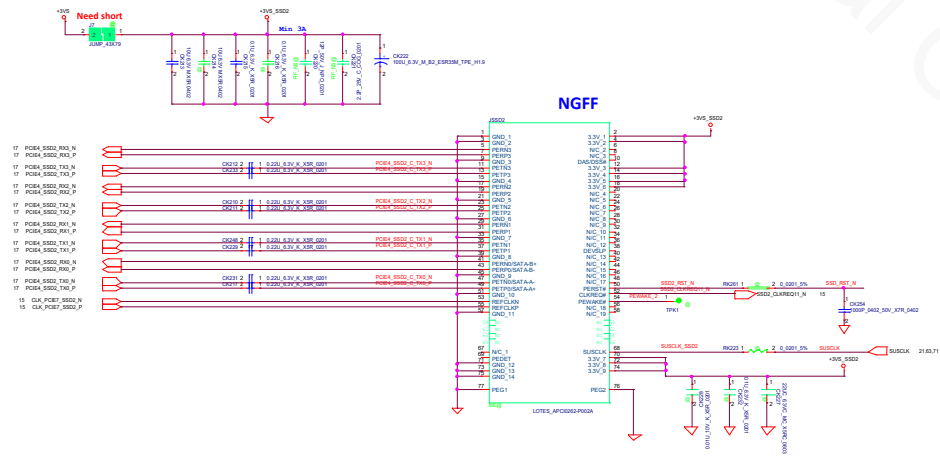
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Date		Issued		2023/07/01	Sheet
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M.2 SSD(PCIE GEN4 from CPU) Main storage



M.2 SSD(PCIE Gen4 from PCH)

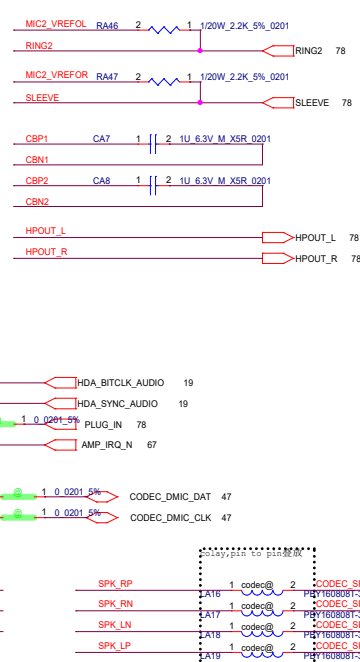
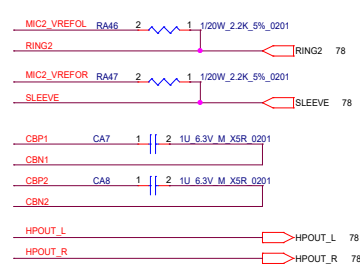
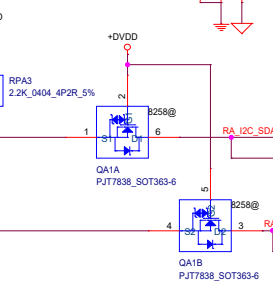
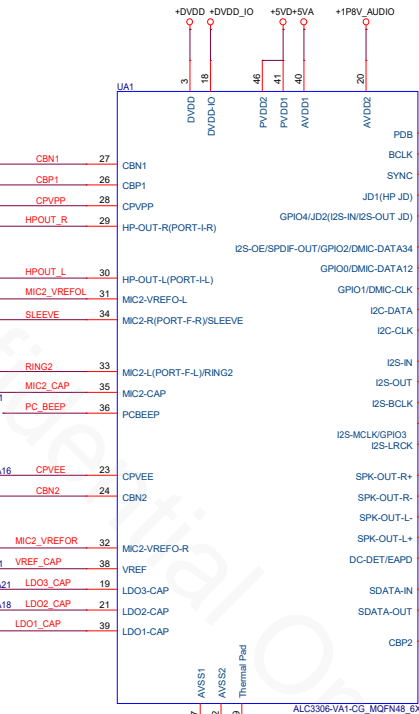
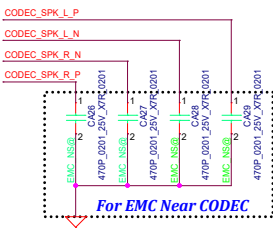
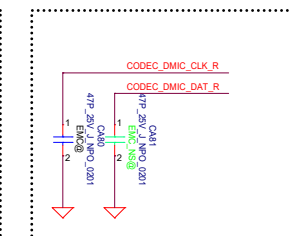
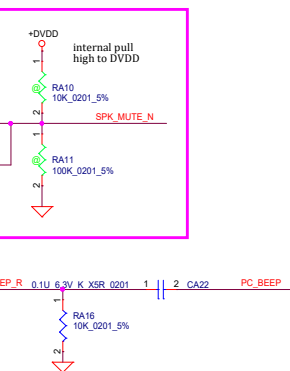
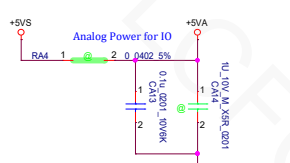
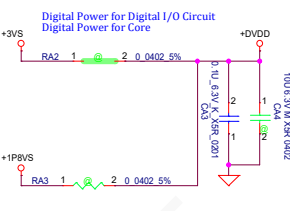


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Rev	D	Document Number	YX801intel		Rev
Date		Issued		2023/07/01	6.1

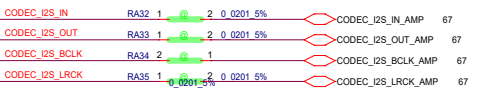
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Codec Only

Codec With Amplifier



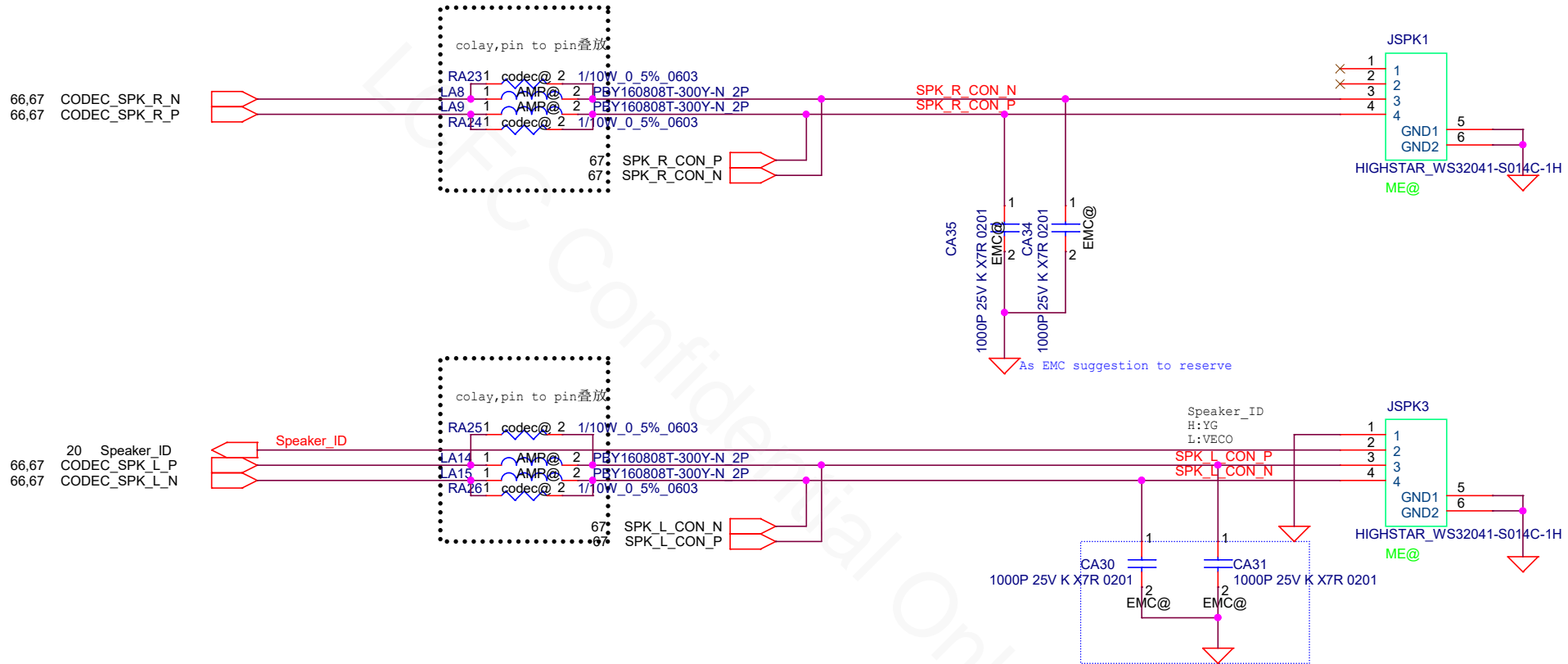
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2022/07/01		2024/07/01					
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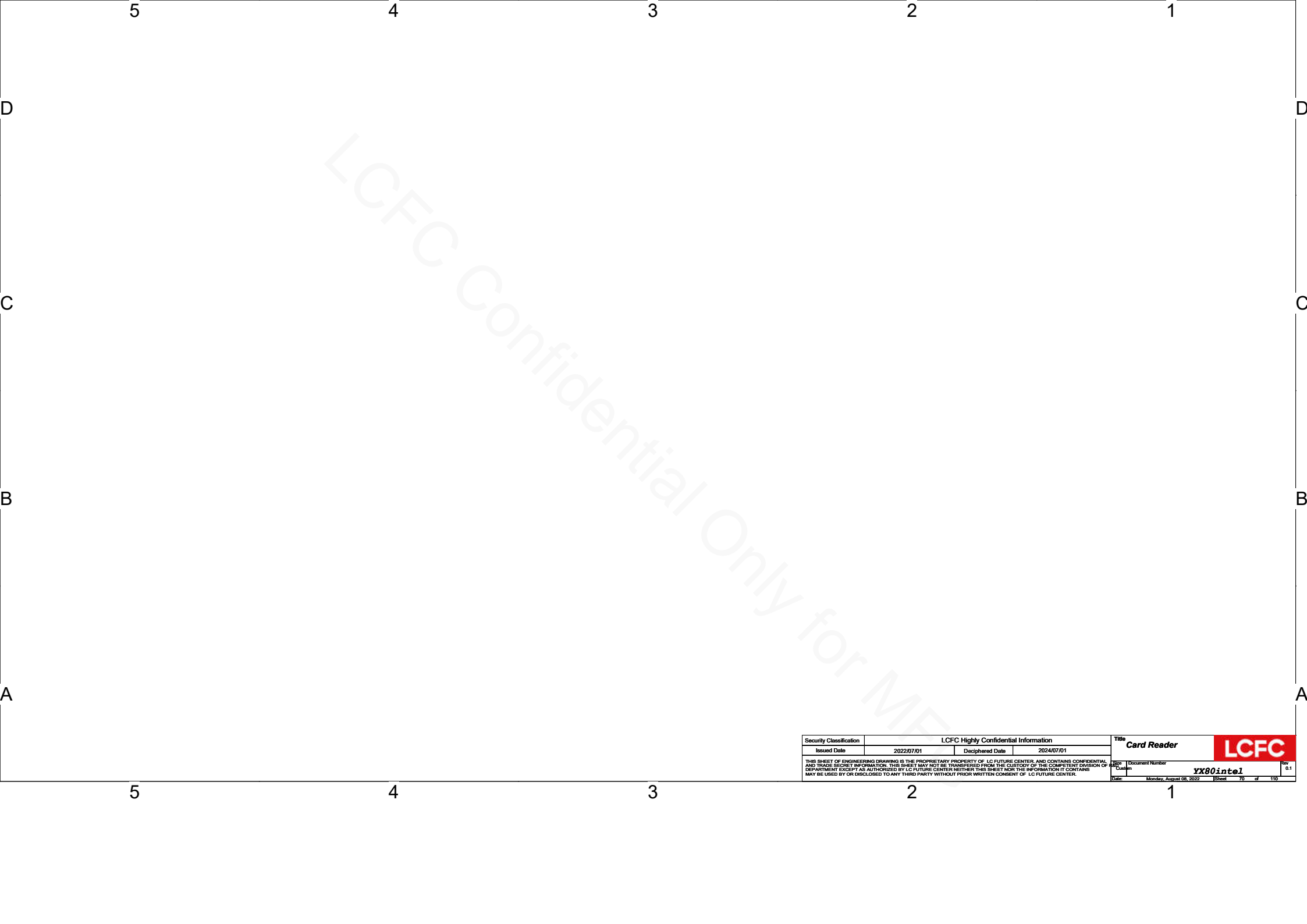
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C	yx80intel				0.1	
Date: Monday, August 08, 2022						
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Speaker

SPK L+ L- R+ R- trace width
Speaker 4 ohm ==> 40 mils
Speaker 8 ohm ==> 20 mils



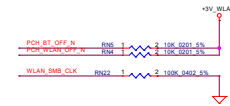
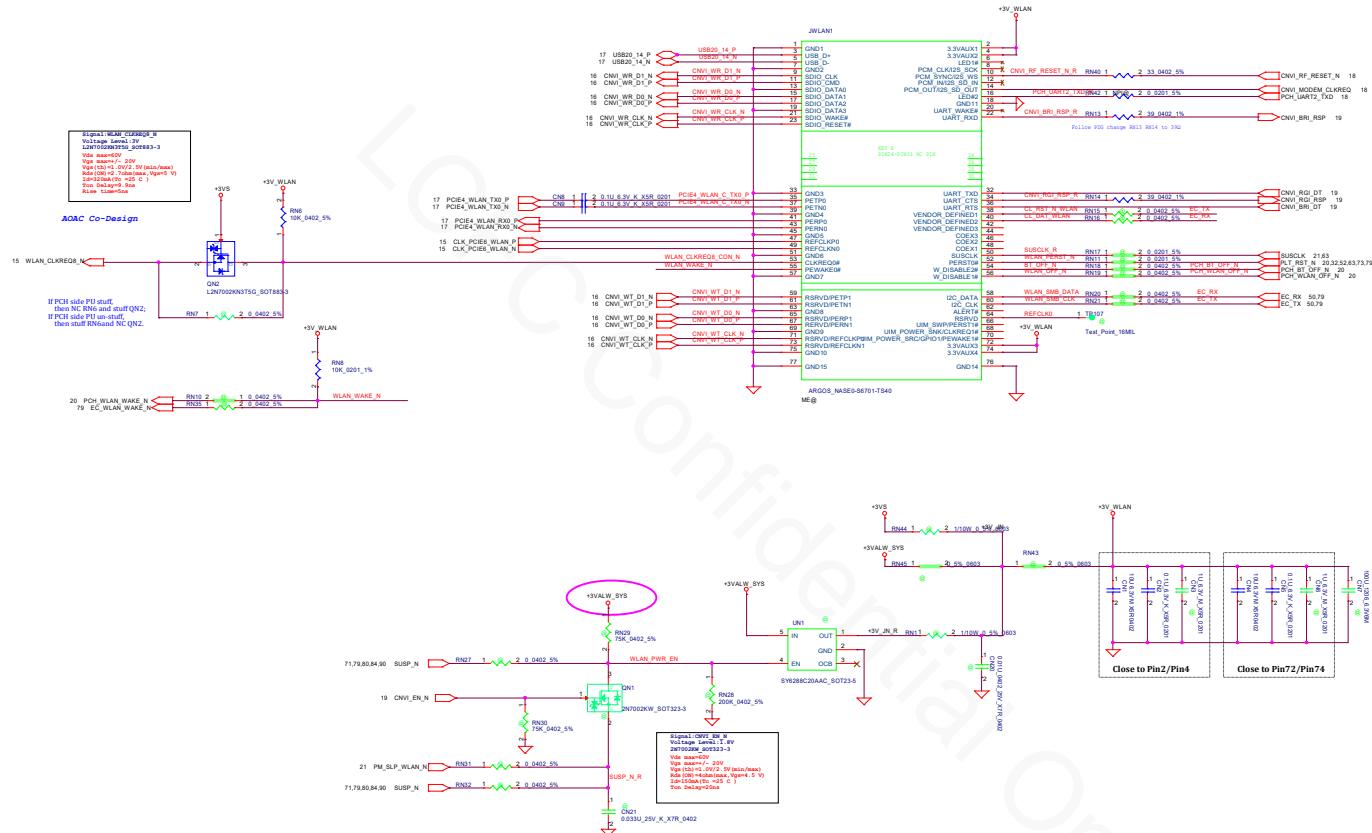
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				Date:	Tuesday, September 13, 2022	Sheet	69 of 110



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				Date	Monday, August 08, 2022
				Sheet	70 of 110



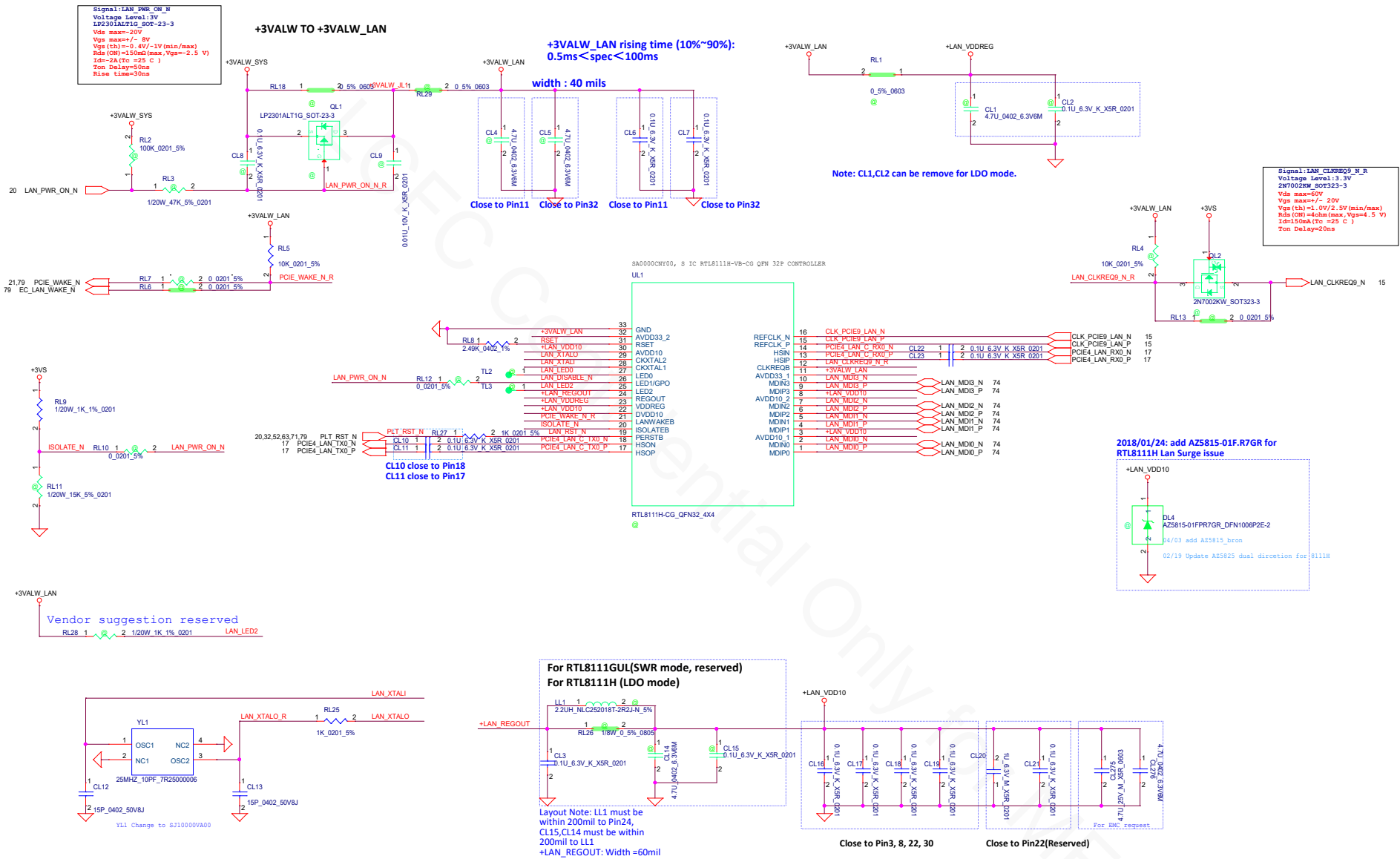
Mini-Express Card(WLAN/WiMAX)

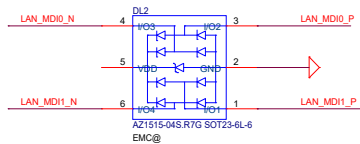


CNV1	
GPP_M4 / CNV_RGI_DT / UART0_TXD	<p>★ This strap does not have an internal pull-up or pull-down. A weak external pull-up is required.</p> <ul style="list-style-type: none"> 0 = Integrated CNVn disabled. 1 = Integrated CNVn enabled.
GPP_D2 / CNV_BRI_DT / UART0_RTSn	<p>★ This strap has a 20 kOhm ± 30% internal pull-up-down.</p> <p>0 = Bit 0 (LSB) of the 2-bit encoded pin straps XTAL Frequency Selection.</p> <p>★ This strap is used in conjunction with XTAL Frequency Selection Bit 1 of GPP_R23 / SIGNALSWP_CSWRT0 pin.</p> <p>2-bit XTAL Frequency Selection encodings:</p> <ul style="list-style-type: none"> 00 = 24 MHz MHz (default) 01 = Reserved *10 = 38.4 MHz *11 = 48 MHz

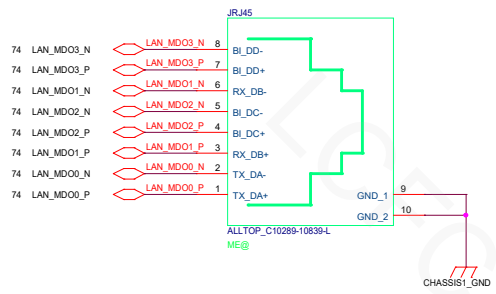
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				1	WLAN081
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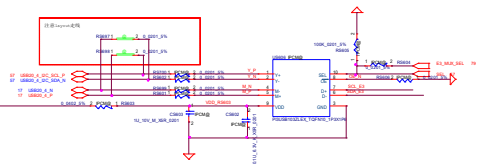
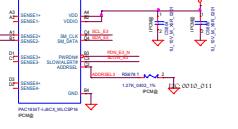
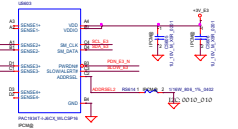
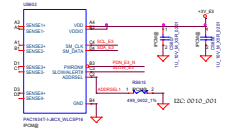
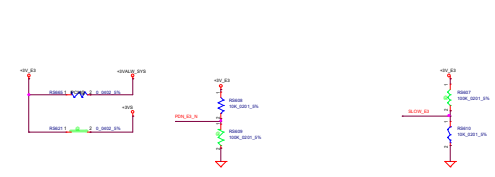
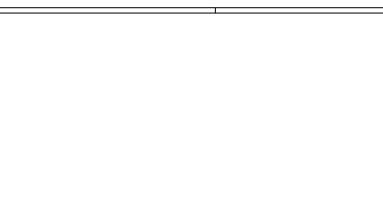
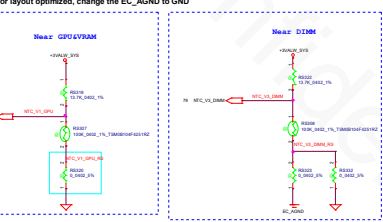
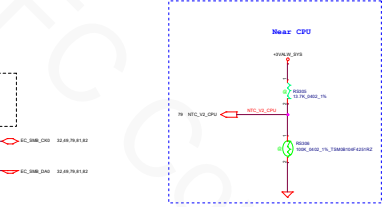
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Date: Wednesday, September 28, 2022										Sheet 74		of 110			

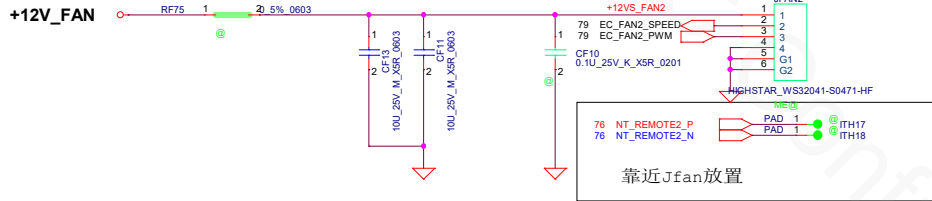




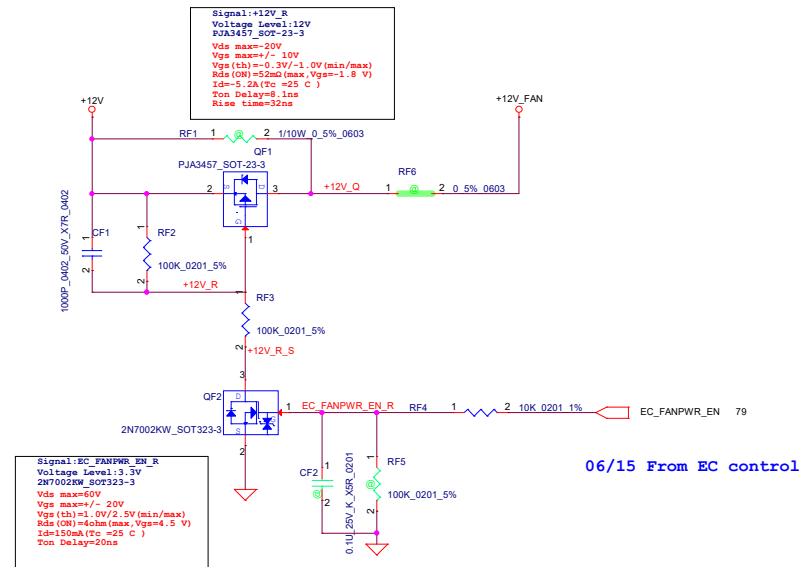
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X	H	H-Z	H-Z
L	L	M+	M-
H	L	D+	D-

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FAN Conn LEFT



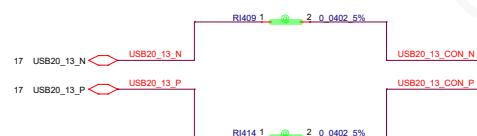
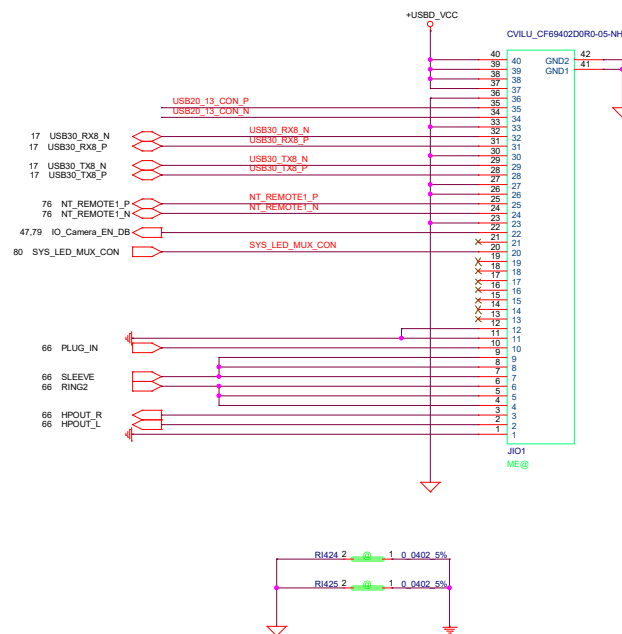
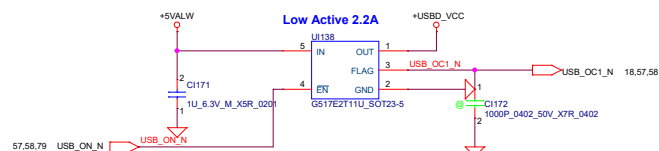
靠近Jfan放置




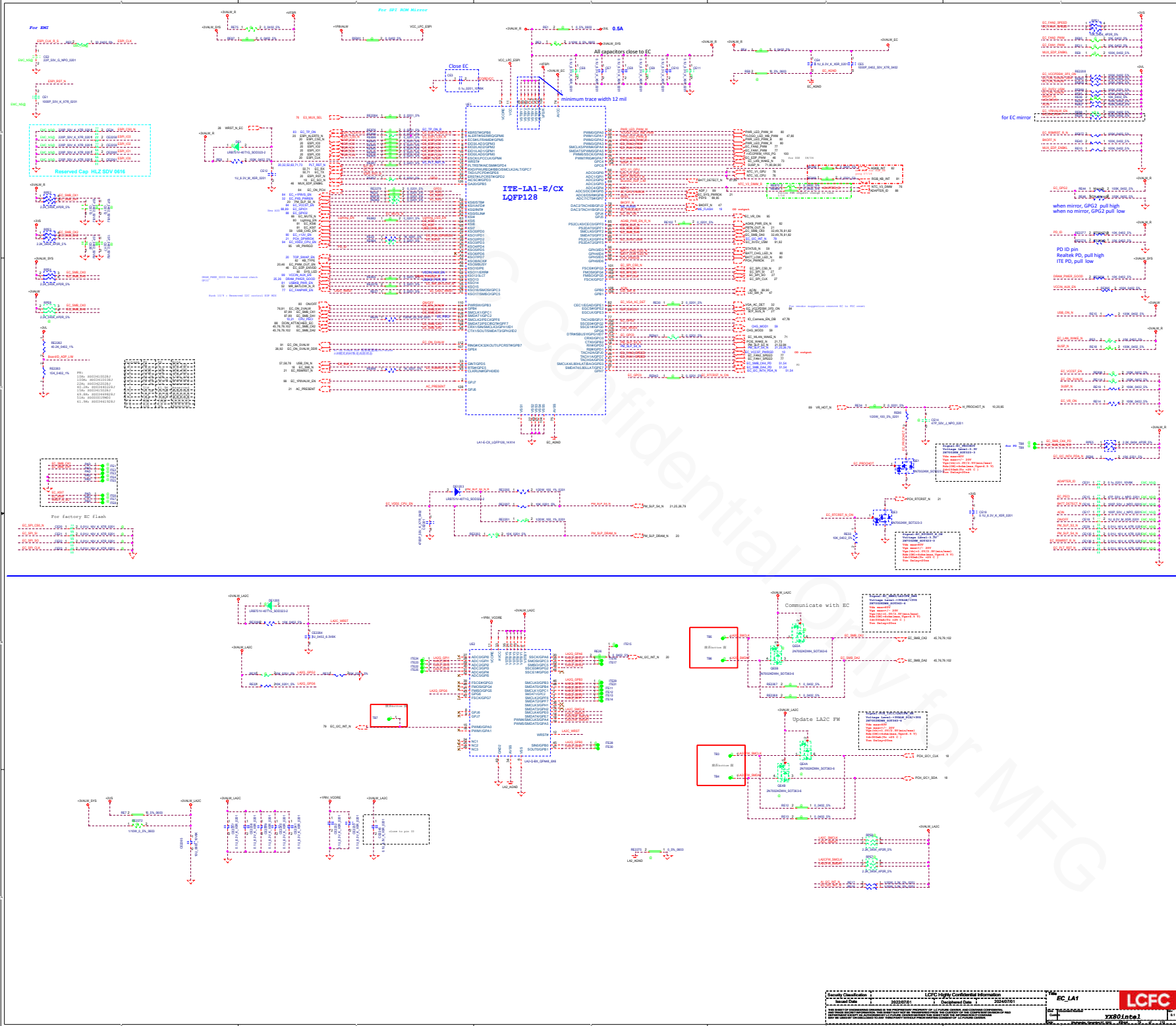
06/15 From EC control

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Issued Date		Deciphered Date		<i>Thermal</i>			
2022/07/01		2024/07/01		Size		Rev	
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				YX80intel			
				Date: Wednesday, November 23, 2022 Sheet 77 of 110			

Right Side USB2.0 Port X 1 (USB/B)

**USB3.1 PORT x1**

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Revision	Document Number	Revision		Revision		Rev
		x90intel				0
Date:	Monday, November 26, 2022		Sheet	26	of	110



for EC mirror

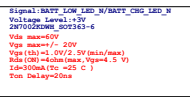
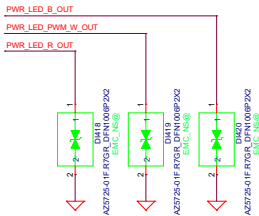
when mirror, GP22 pull high
when no mirror, GP22 pull low

PD ID pin
Realtek PD, pull high
ITE PD, pull low

S	Z
H	Y1
L	Y0

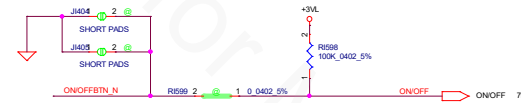


PWR_LED_B_OUT	R8406	1		2	330 0402 1%	LED_B
PWR_LED_PWM_W_OUT	R8407	1		2	1K 0402 1%	PWM_W
PWR_LED_R_OUT	R8408	1		2	220 0402 1%	LED_R

[illegible]

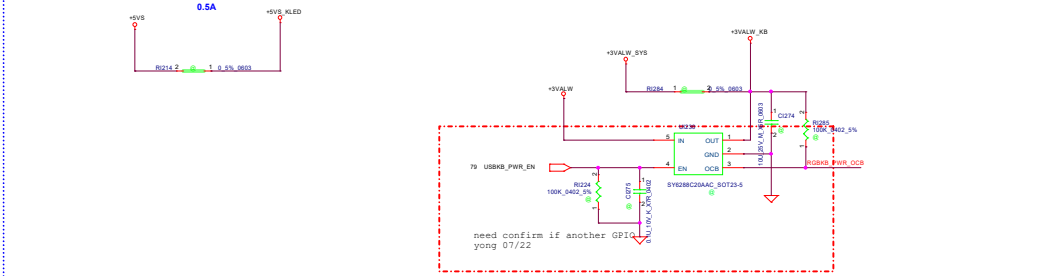
PWRBTN need change to SN10000C700

remove NOVO button

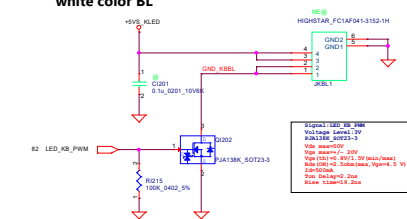


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<p>Saturday, November 26, 2022 18:00</p>				<p>8 of 110</p>	

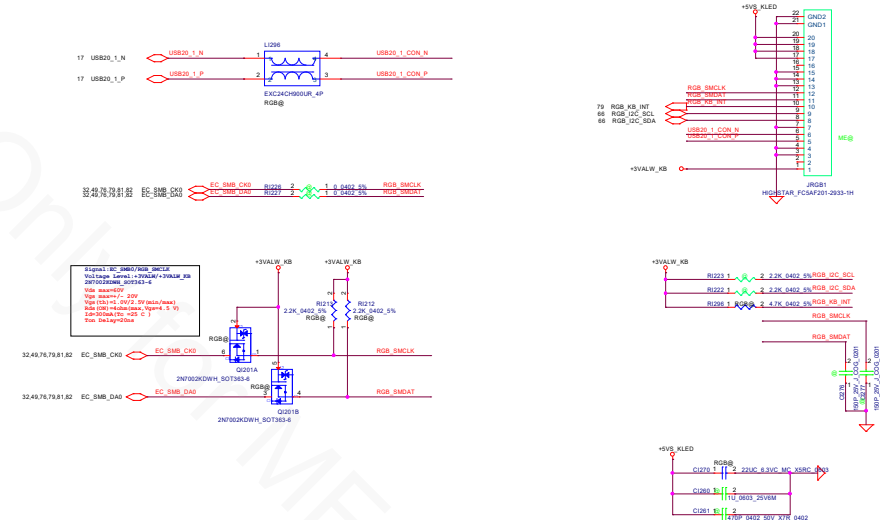
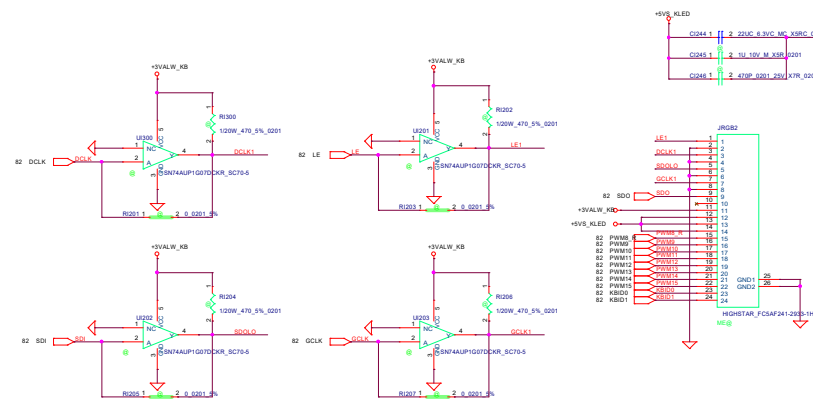
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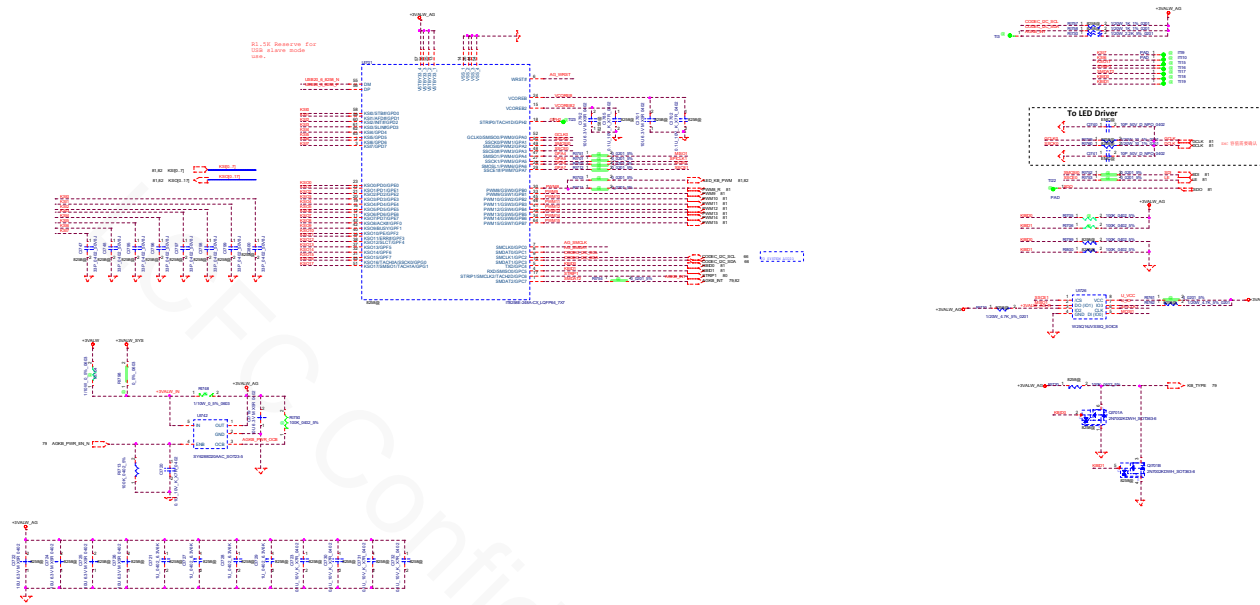
white color BL



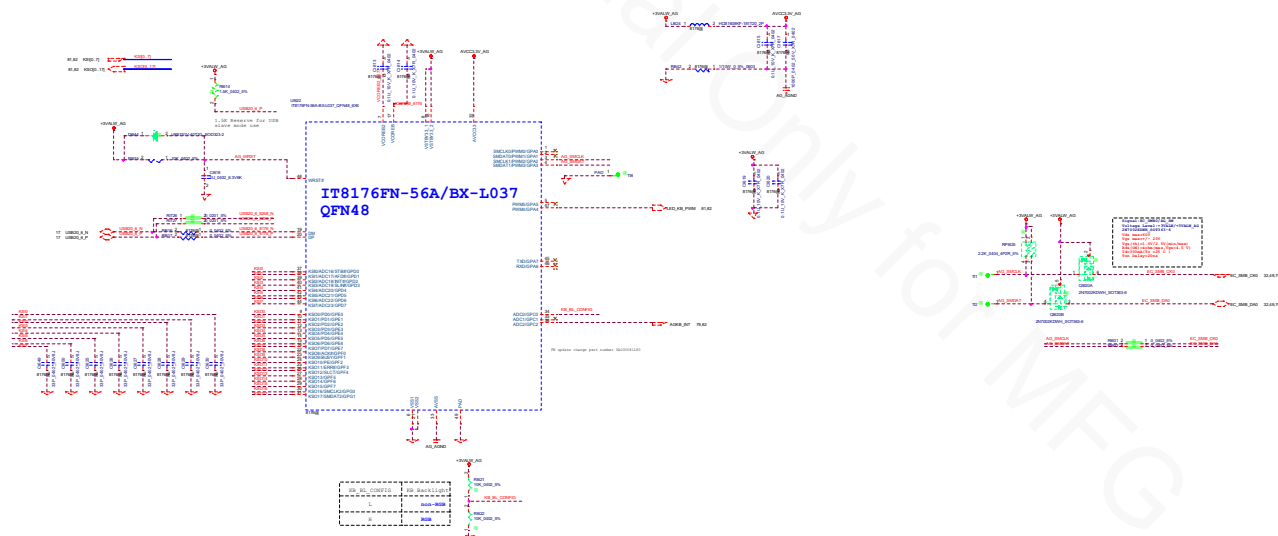
KB lighting 4 zone RGB for Y5
04/27

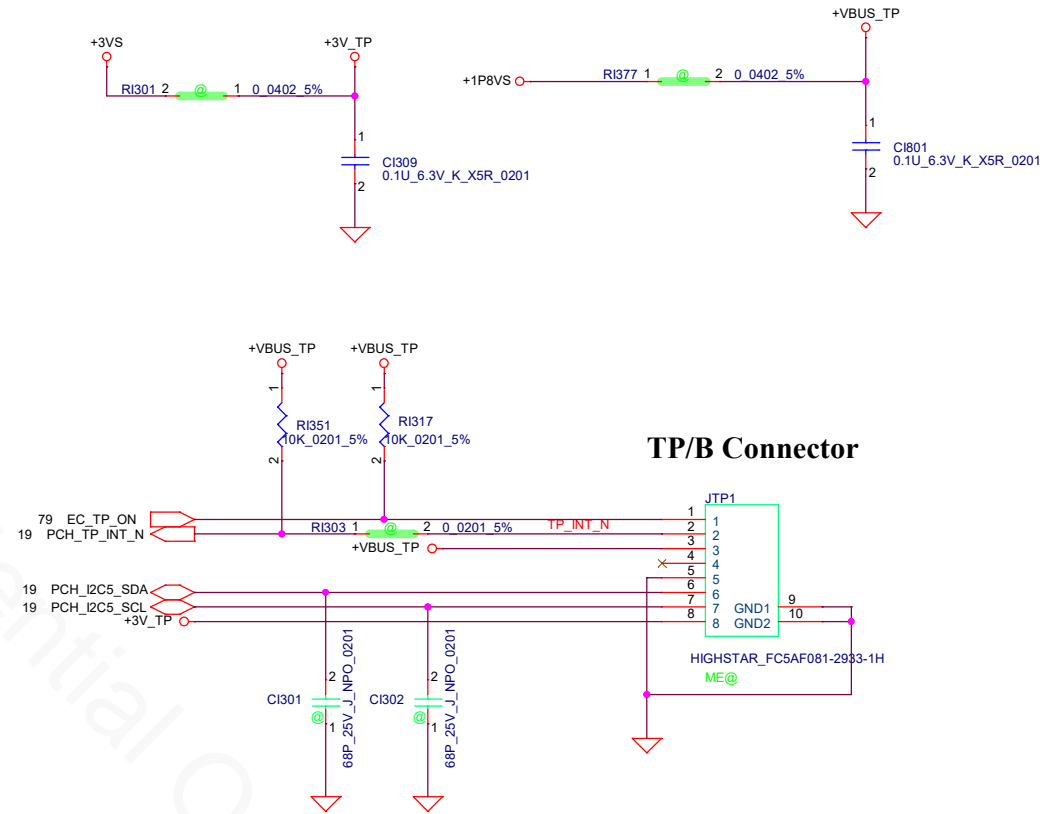
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IT8258

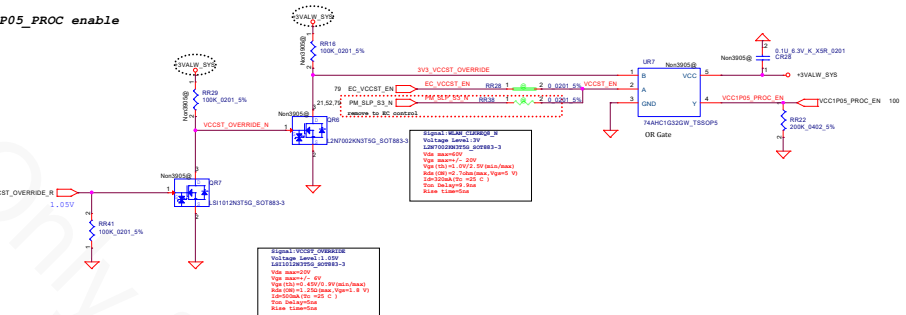
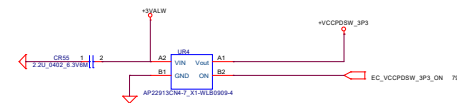


IT8176





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19.99 VCCIN_AUX_PCH_VID0 VCC1P8A_LDO_EN 99

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Date	Document Number	X80intel		
	Issue Number			

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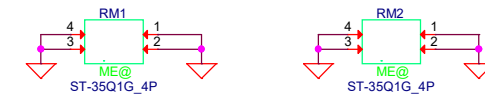
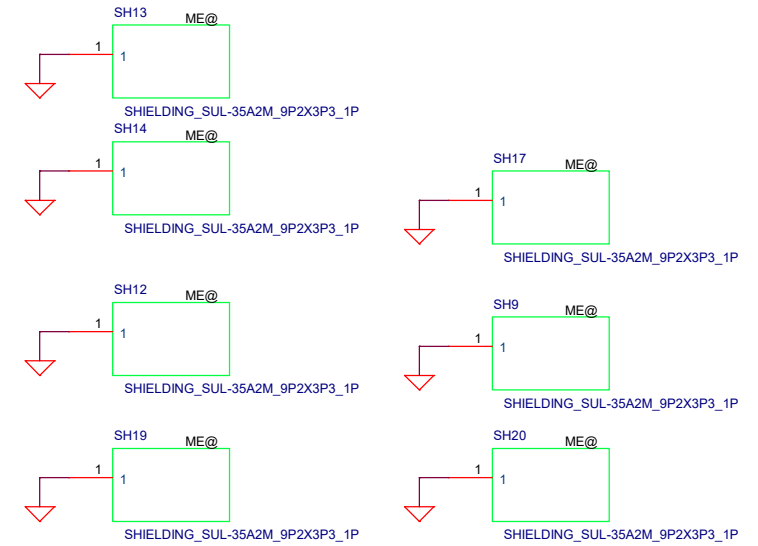
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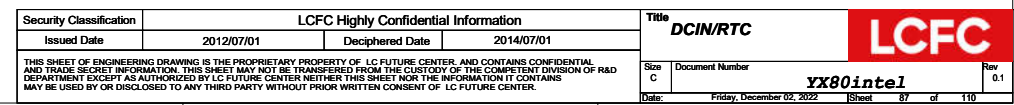
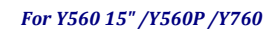
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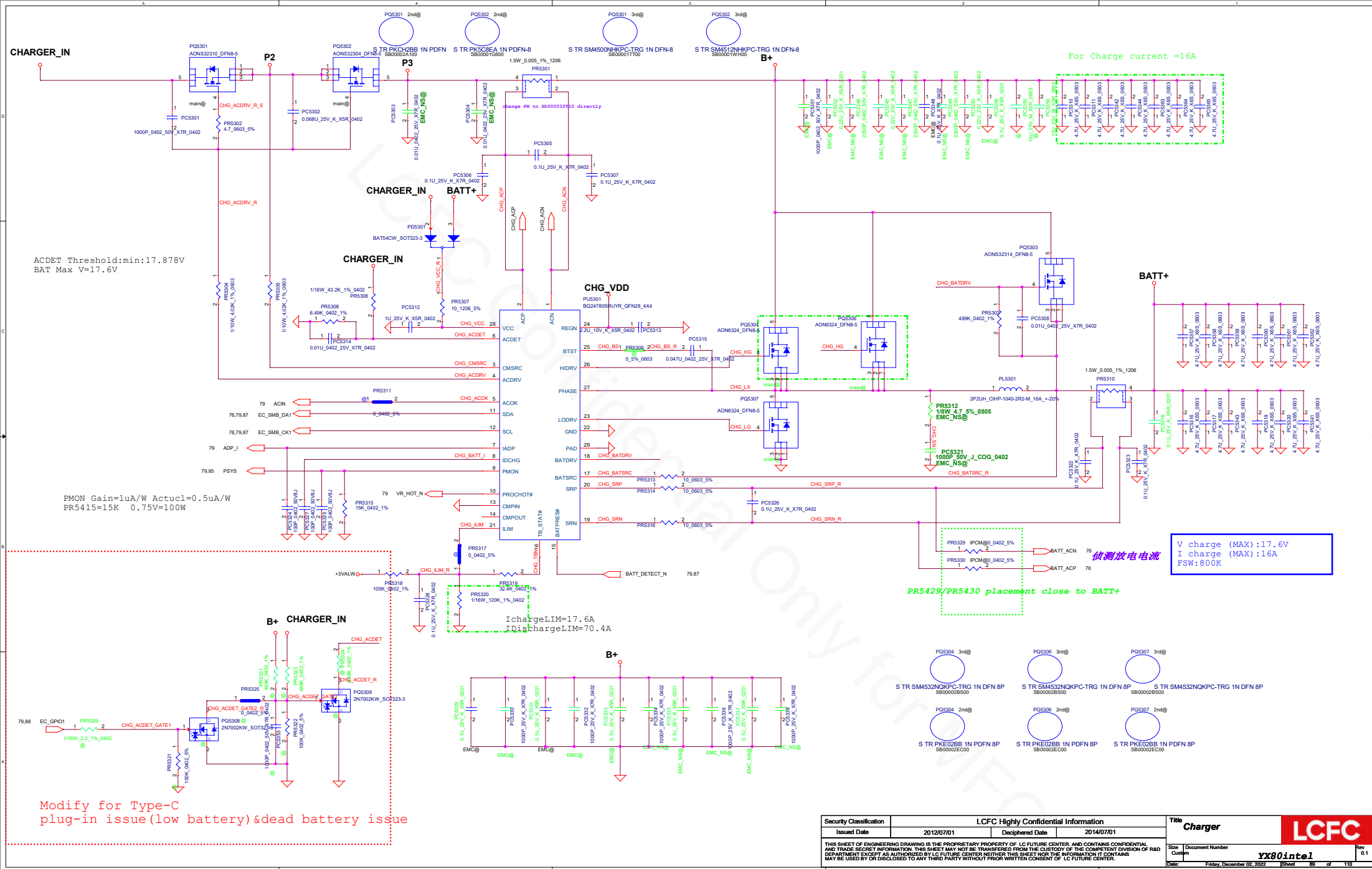
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				Date:	Monday, August 08, 2022	Sheet	85	of	110

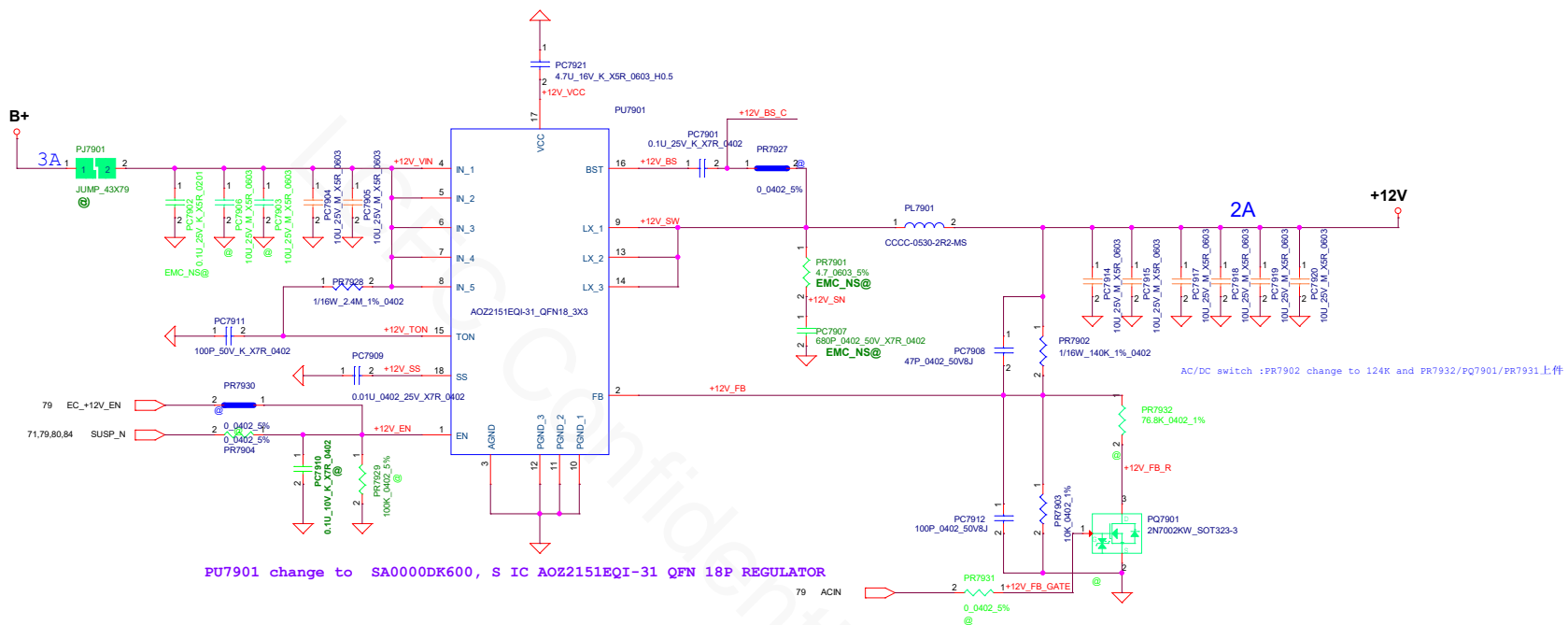
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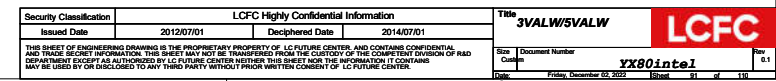


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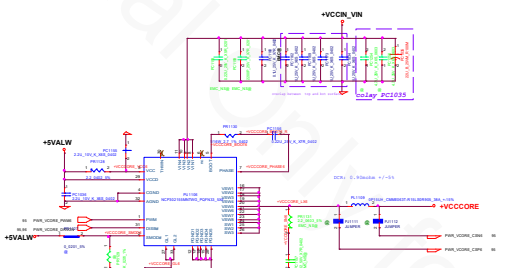
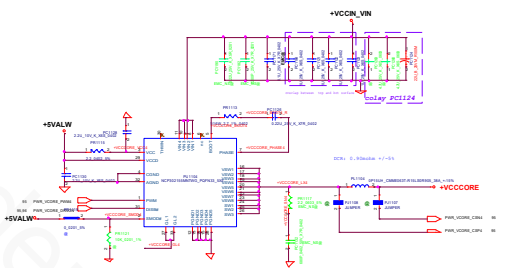
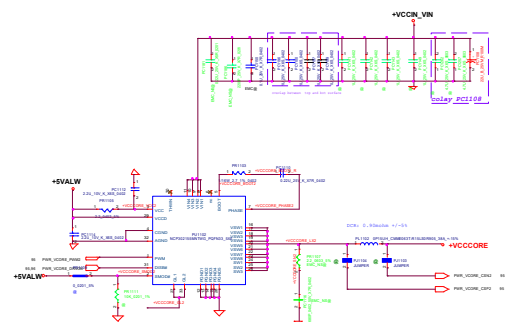






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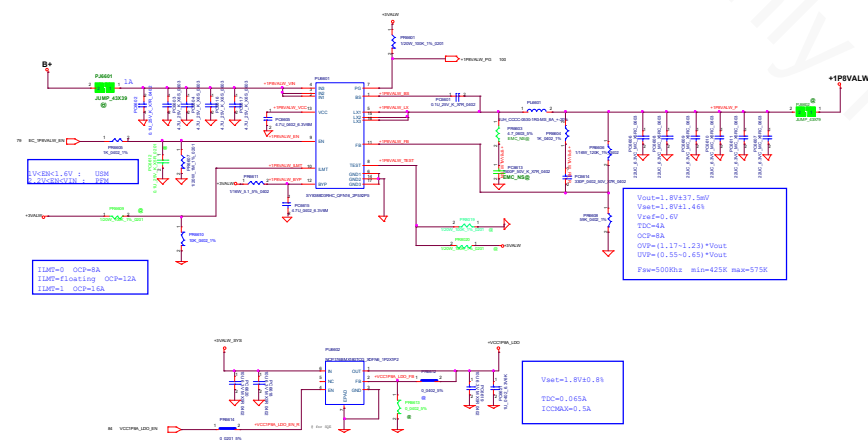
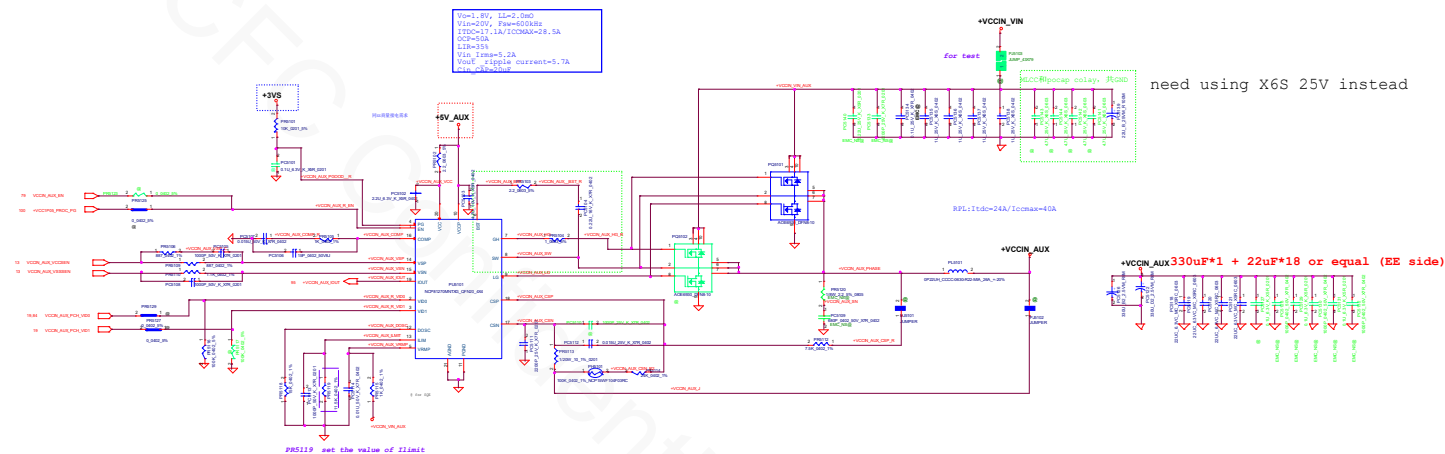
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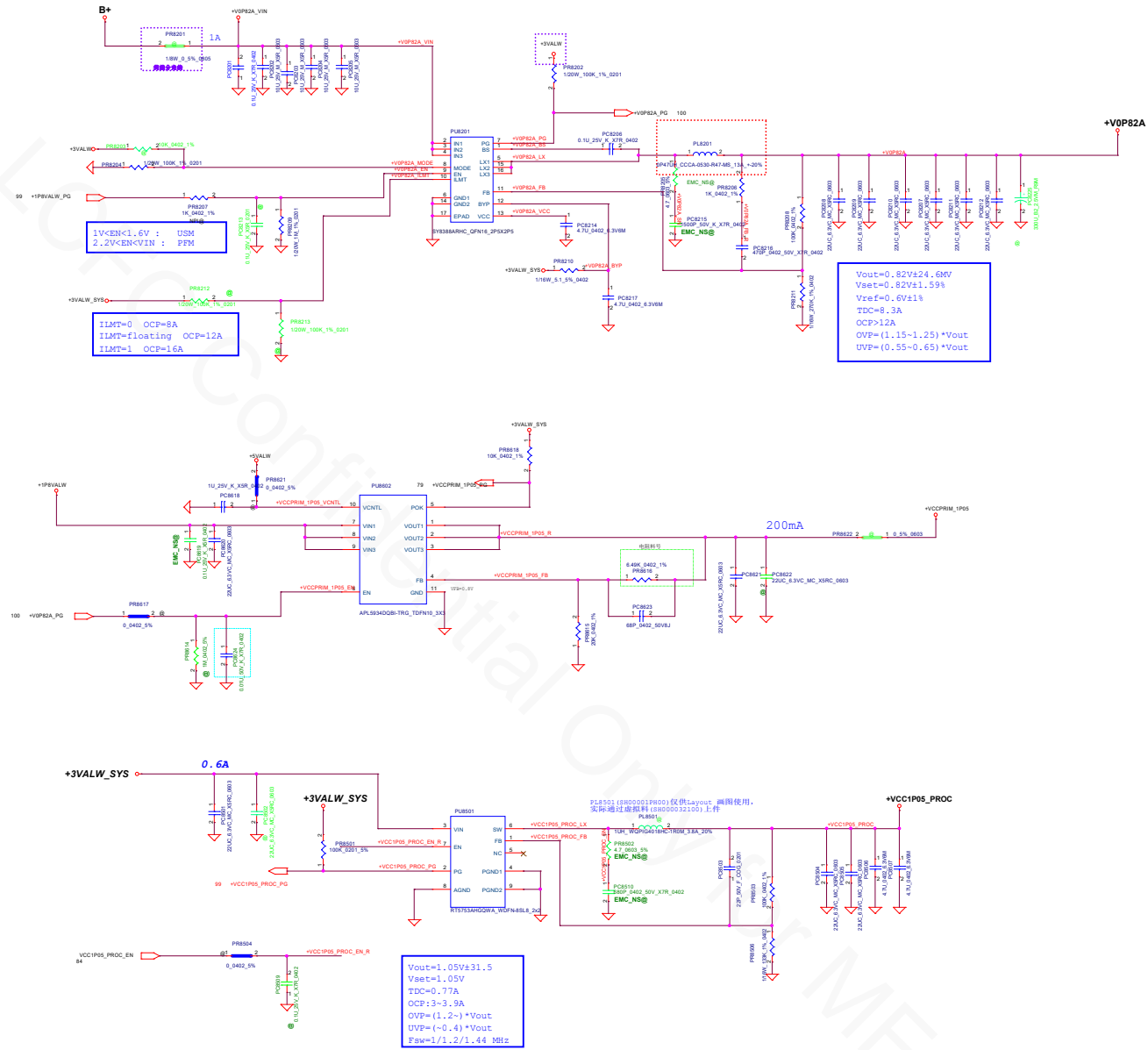


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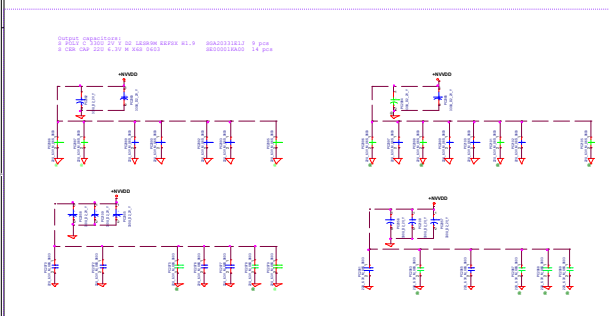
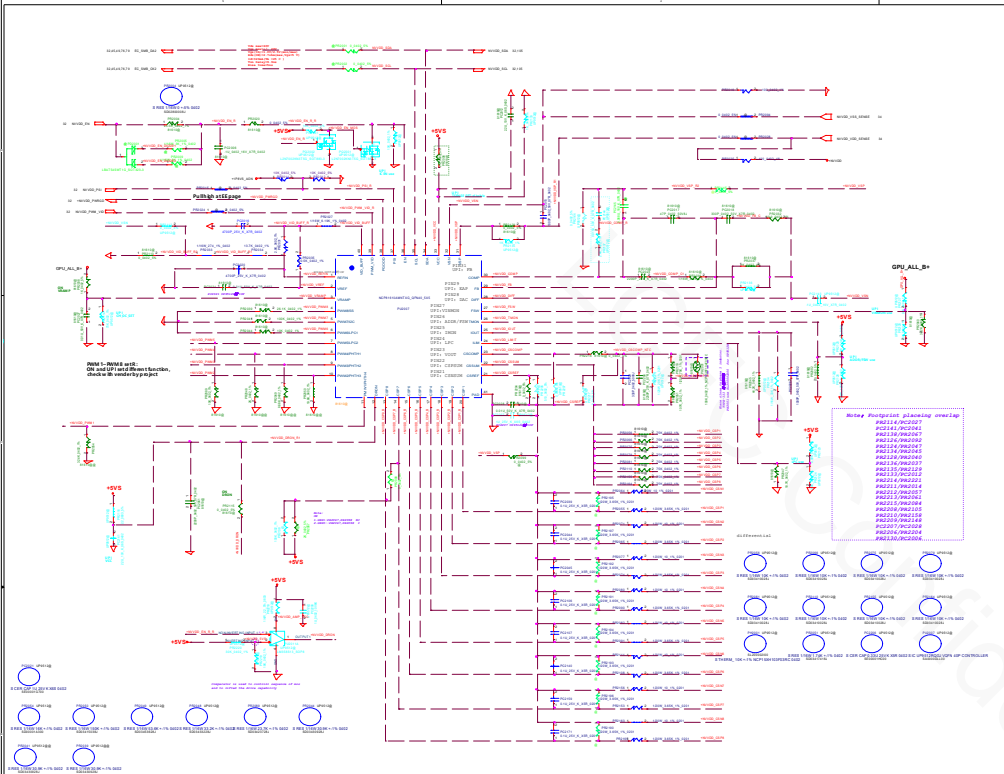
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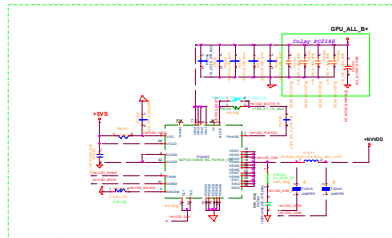
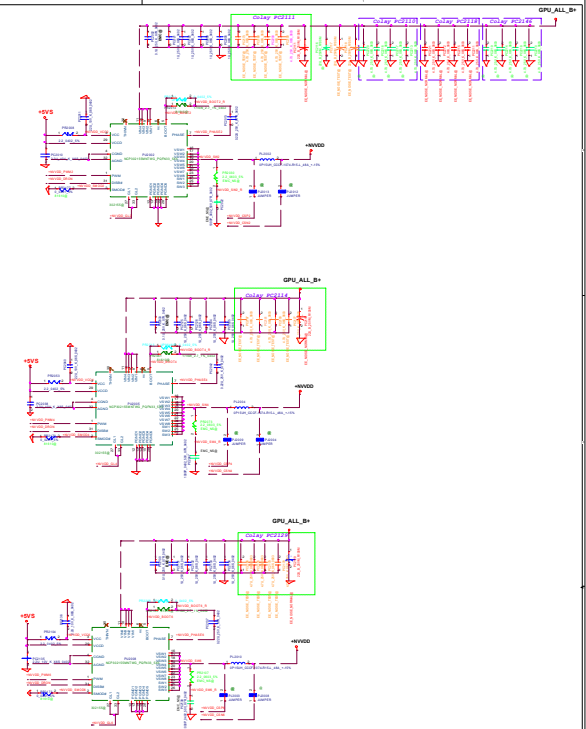
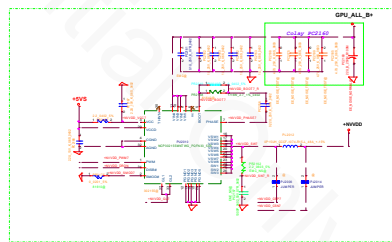
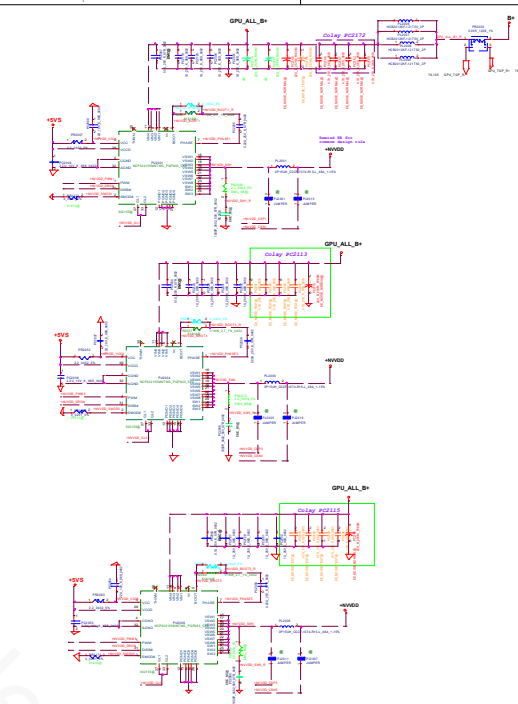


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note:
 1. NVVDD 输出电感L的tolerance 为15%
 2. GN21 use 8 phase 0.15uH SH00003AB00
 3. GN20-E (150W+25W): EDPc=189A, EDPp=525A, 8Phase;
 GN21-E (150W+25W): EDPc=189A, EDPp=525A, 8Phase;



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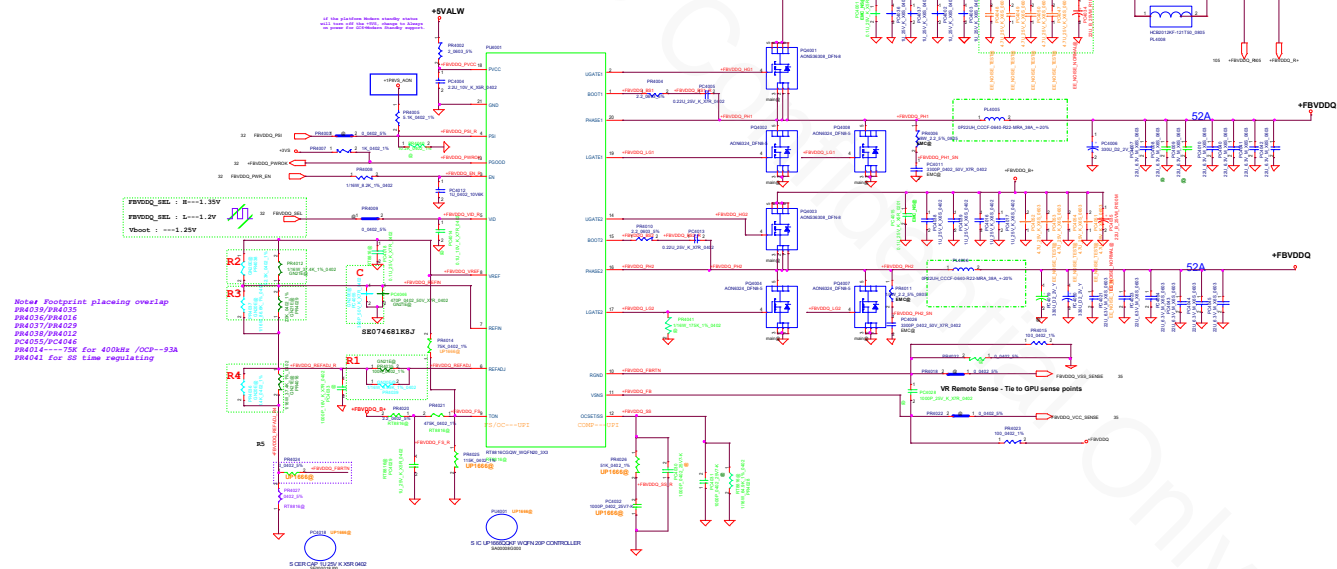
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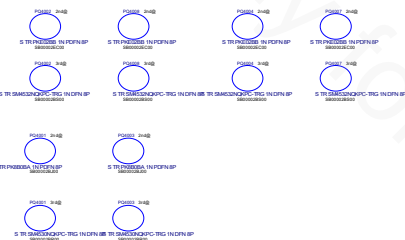
RT8816 PSI	UP1666 PSI	Phase Configuration
1.6V~5.5V	1.6~3.5V	2Phase CCM
1.0V~1.375	2~3.4V	2Phase CCM
0.7~0.88V	0.4V~0.8V	1Phase CCM
0~0.4V	0~0.2V	1Phase CCM

need using X6S 25V instead



Note: Footprint placing overlap
 PR4039/PR4035
 PR4036/PR4036
 PR4037/PR4029
 PR4038/PR4032
 PR4039/PR4036
 PR4040---75K for 400mV /OCP---93A
 PR4041 for SS time regulating

Note:
 FBVDDQ output 2 state Vmin/Vboot/Vmax=1.25V/1.25V/1.35V R1=9.09K/R2=52.3K/R3=86.4K/R4=1.4K/C=300p
 FBVDDQ output 3 state Vmin/Vboot/Vmax=1.2V/1.25V/1.35V R1=100K/R2=25.5K/R3=20K/R4=23.2K/C=480p



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